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VOICE OF THE ENGINEER

JUNE 12

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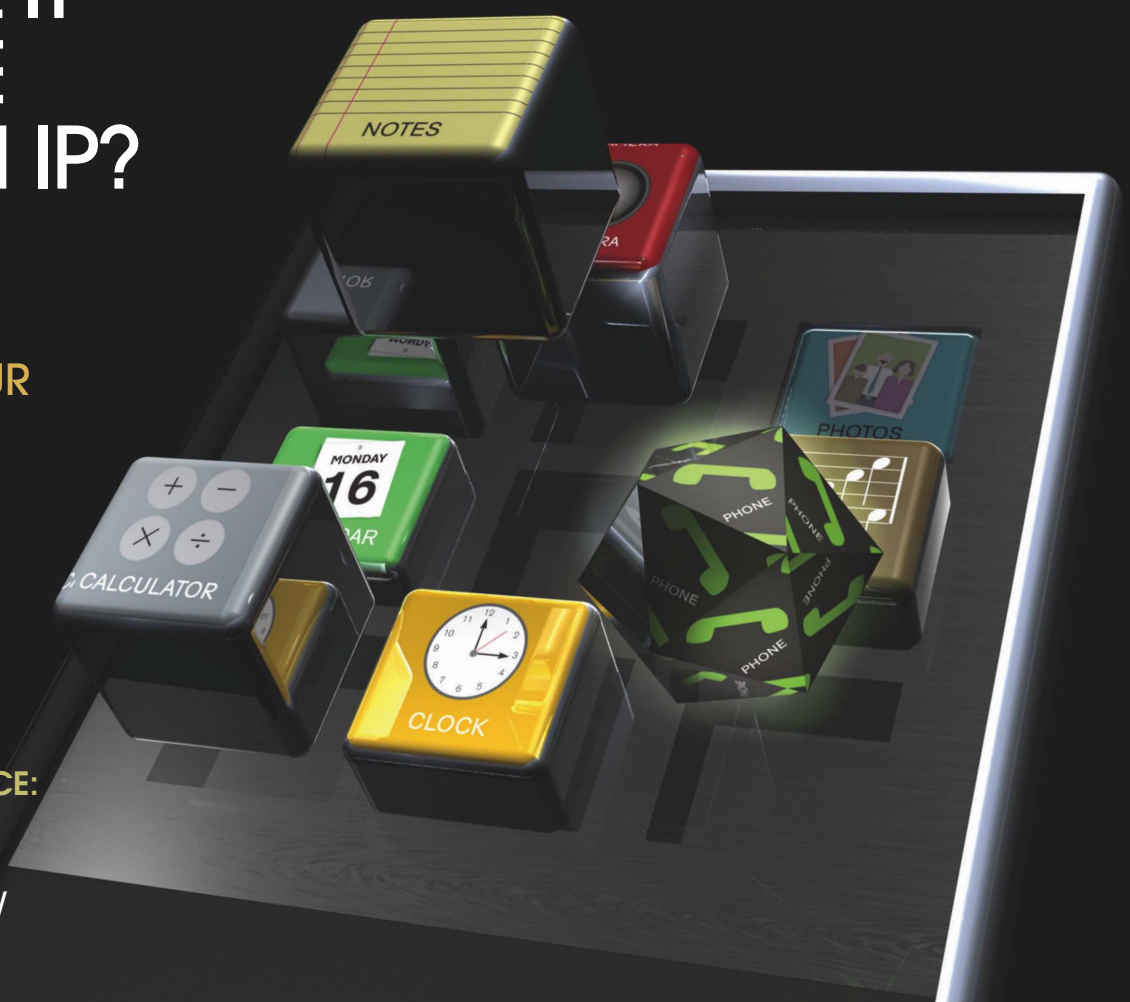

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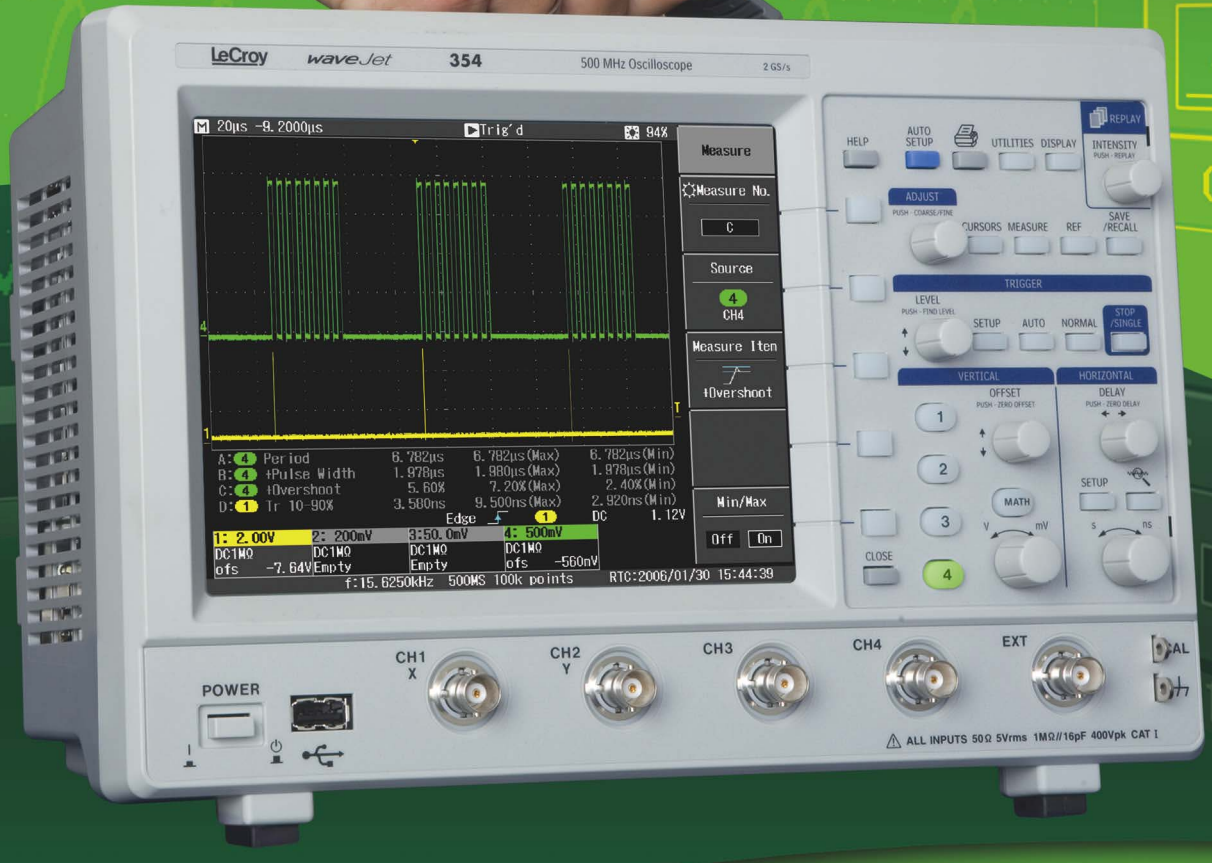

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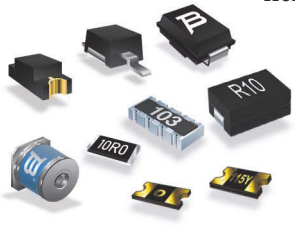

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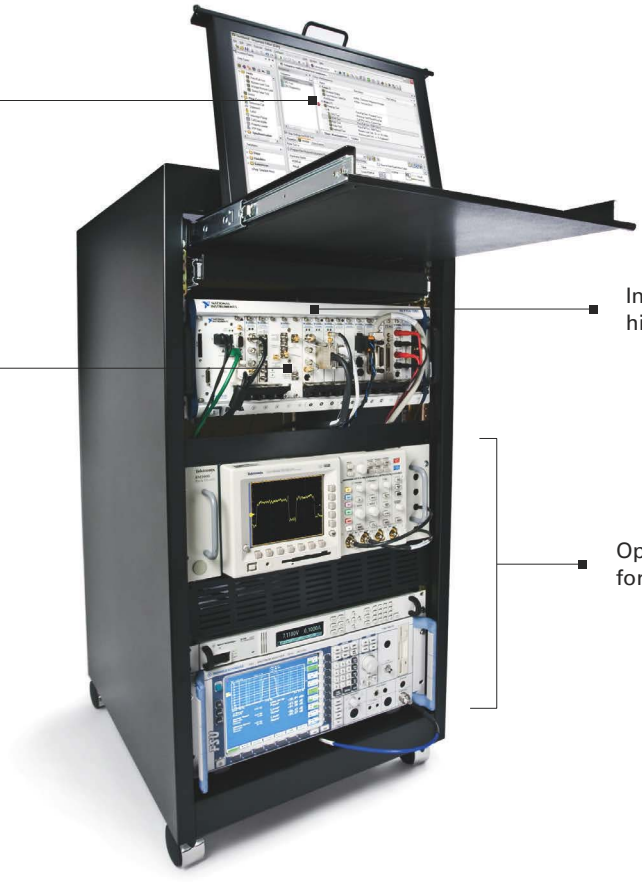

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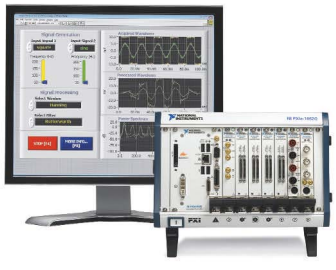

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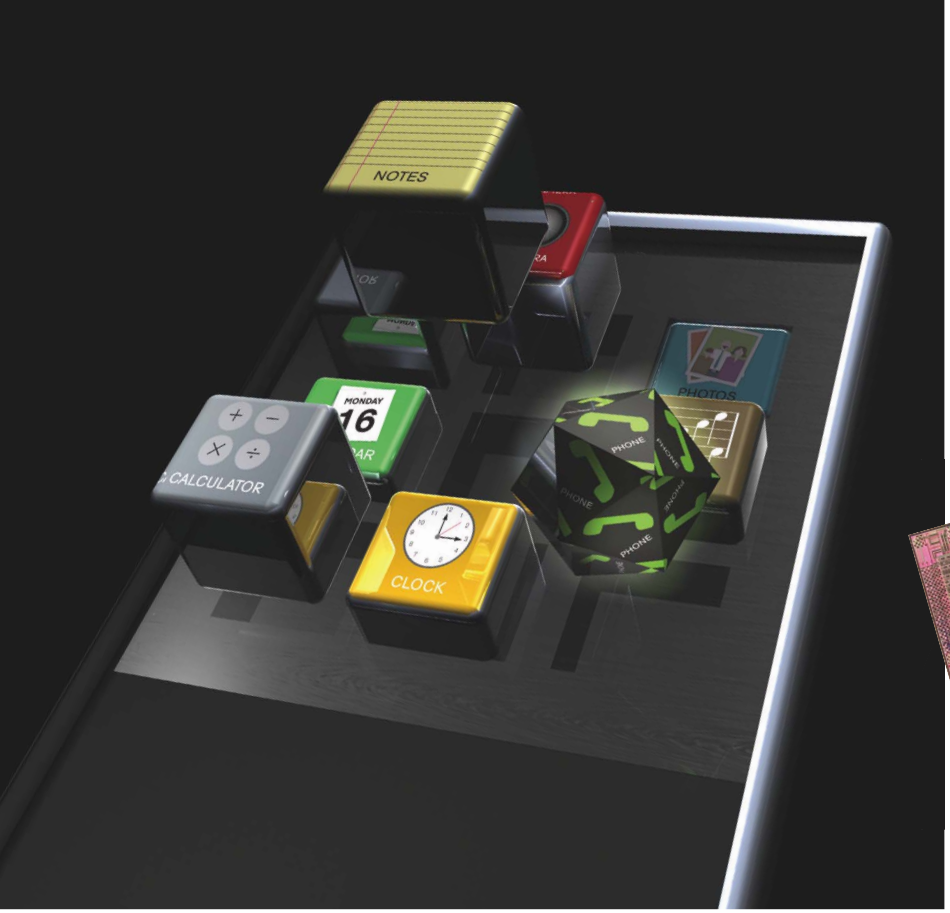

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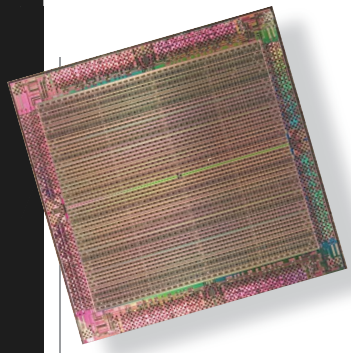

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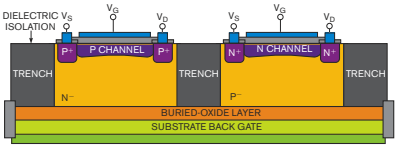

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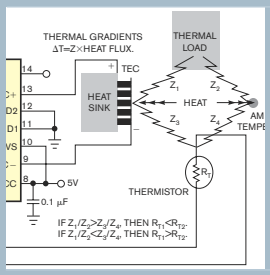

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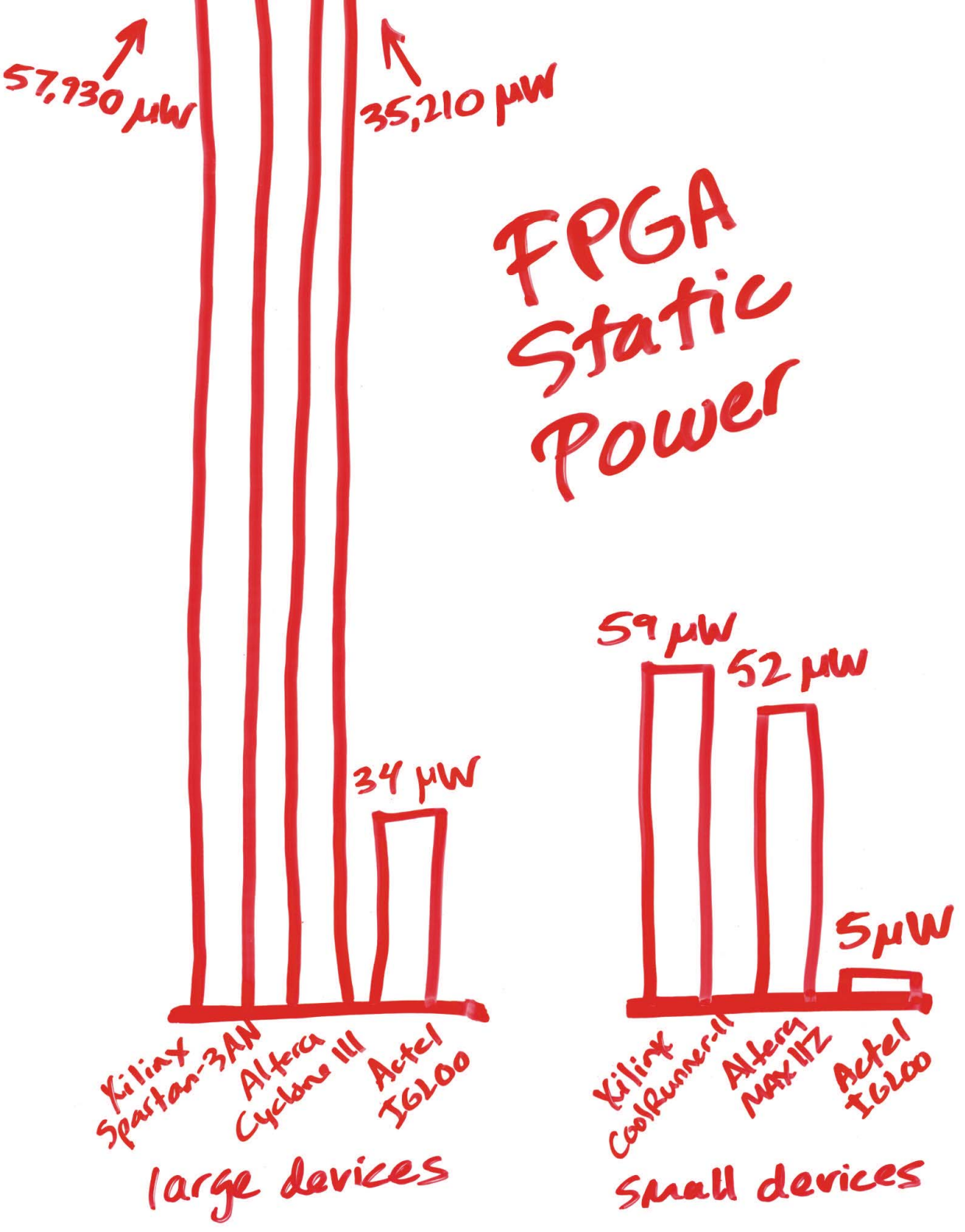

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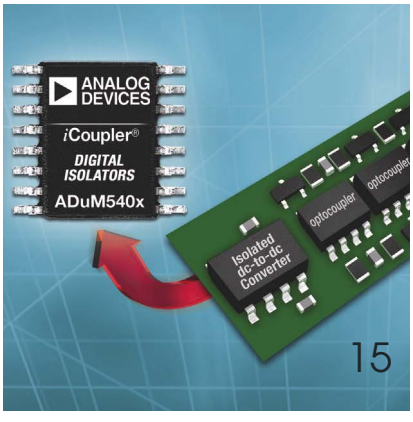

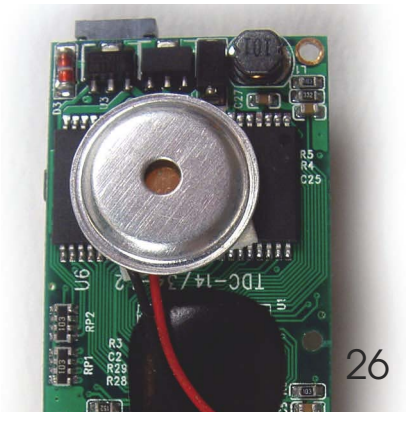

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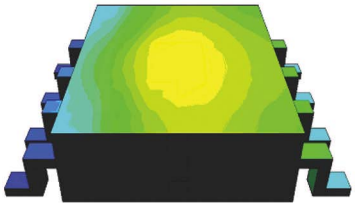

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How to kill the home-networking industry

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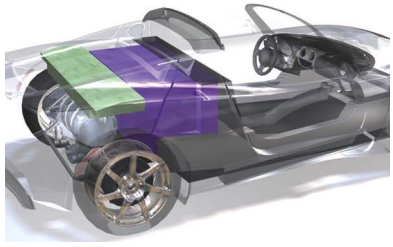

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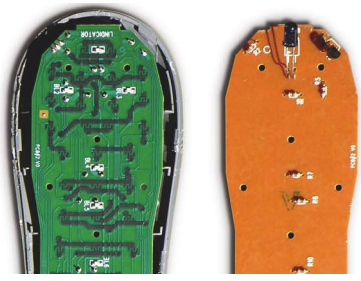

PRYING EYES

An inside look at design decisions

In Prying Eyes, we peer inside an end-user gadget, a reference design, or any other interesting electronics-enabled thing we can get a good look at. Unlike your average bill-of-materials teardown, Prying Eyes aims to illuminate the tough design decisions the engineers responsible for the design had to make. Check out this issue's installment on pg 26 and then visit the complete online Prying Eyes archive.

→www.edn.com/pryingeyes

FROM *EDN*'S BLOG

PC support: For want of a simple sticker, the profit was lost

From Brian's Brain, by Brian Dipert

Can you guess what perfectly understandable and (I suspect) common hookup snafu Lisa had made? She mated the display to the integrated graphics connector, not to the output of the stand-alone graphics card.

→ www.edn.com/080612toc7

BY PAUL RAKO, TECHNICAL EDITOR

Fear of feature-itis

I recently bought an Olympus DS-30 digital-voice recorder that comes with an 86-page manual, a typical example of "feature-itis"—a bewildering array of too many useless features. Consumer-electronics manufacturers believe that feature-itis makes their products more desirable, and some of the features of the DS-30 are in fact desirable. For example, it operates from two AA batteries. The last thing I want is some product that I would have to plug into a USB port for an hour to use.

Looking at all the switches and buttons on the recorder only intensified my regret at seeing the manual fall out of the box. The recorder has three positions for microphone sensitivity. It has a power switch and a hold switch. It has play, stop, and record switches. It has an erase button. It has three software-defined buttons under the LCD. It has five more buttons in a circular-navigation array. OK, here is what I wanted: one toggle switch. When the switch is up, the recorder is on. When the switch is down, the recorder is off.

These days, modern consumer-electronics devices must be little computers. They have to boot up. And the tiny LCD must show all the folders in which I could file my recordings. The designers and marketers at Olympus apparently think that I want to spend my time arranging files into folders with five little buttons and a 1-in. LCD screen. On the contrary, I am not going to store my precious recordings on a little gizmo the size of a couple of matchbooks. The Olympus designers apparently forgot that I could lose this recorder, or someone could steal it.

Maybe teenagers like these little gizmos with a zillion functions, but I need a tool, not a toy.

The real-use scenario is that, 20 minutes after I make a recording, I put it on my workstation, and a few minutes later, I back up those files on a second machine and a USB drive. Later in the week, I swap that USB drive with one in my safe-deposit box. I do any file arranging on my dual Dell 24-in. monitors using a 104-key keyboard and a three-button mouse with a scroll wheel.

Maybe teenagers like these little gizmos with a zillion functions, but I need a tool, not a toy.

I needed the recorder for an interview with frequent *EDN* contributor Jim Williams, staff scientist at Linear Technology, and I bought the device on my way to see him. I had no time to research the purchase. Once I had the time, I looked at comments about the recorder on the Internet, and I saw that, with all these features, the D-30 still lacked the one thing that might be useful: the ability to rewind for a few seconds and then rerecord, meaning that you can't use it to dictate letters or articles, as you could with any Dictaphone that debuted since 1959.

Giant manuals and tons of useless features bring to mind the old Logitech-mouse days. All we wanted back then was a pointing device. Logitech came with a big manual and all kinds of software, some of which was evil TSR (terminate-and-stay-resident) programs that ate up memory and caused a host of incompatibilities and problems. You see, Logitech had a big department for designing mice, and that team was going to keep adding features that nobody wanted.

Here's another example of feature-itis: I recently needed a stud sensor to help me mount a whiteboard on a wall. I borrowed a simple Zircon model from a friend. It had one LED that turned on when you slid it past a stud. I was so impressed that I went out and bough a Zircon of my own. The store didn't have the basic $8 model, so I bought the full-featured $29 model. It was supposed to do "deep sensing" and find wires in walls. It came with a CD instruction manual. But it didn't work. It had 10 flashing LEDs, but it could not reliably find the stud like the sister product that cost approximately $20 less. It looked to me like a clear case of feature-itis, so I took it back and found the $8 one at another store.EDN

Contact me at paul.rako@edn.com.

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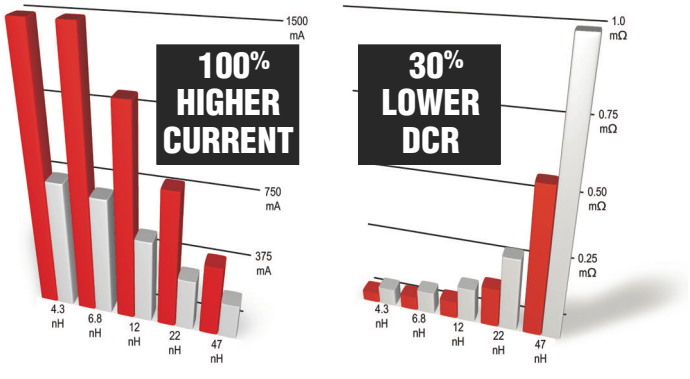

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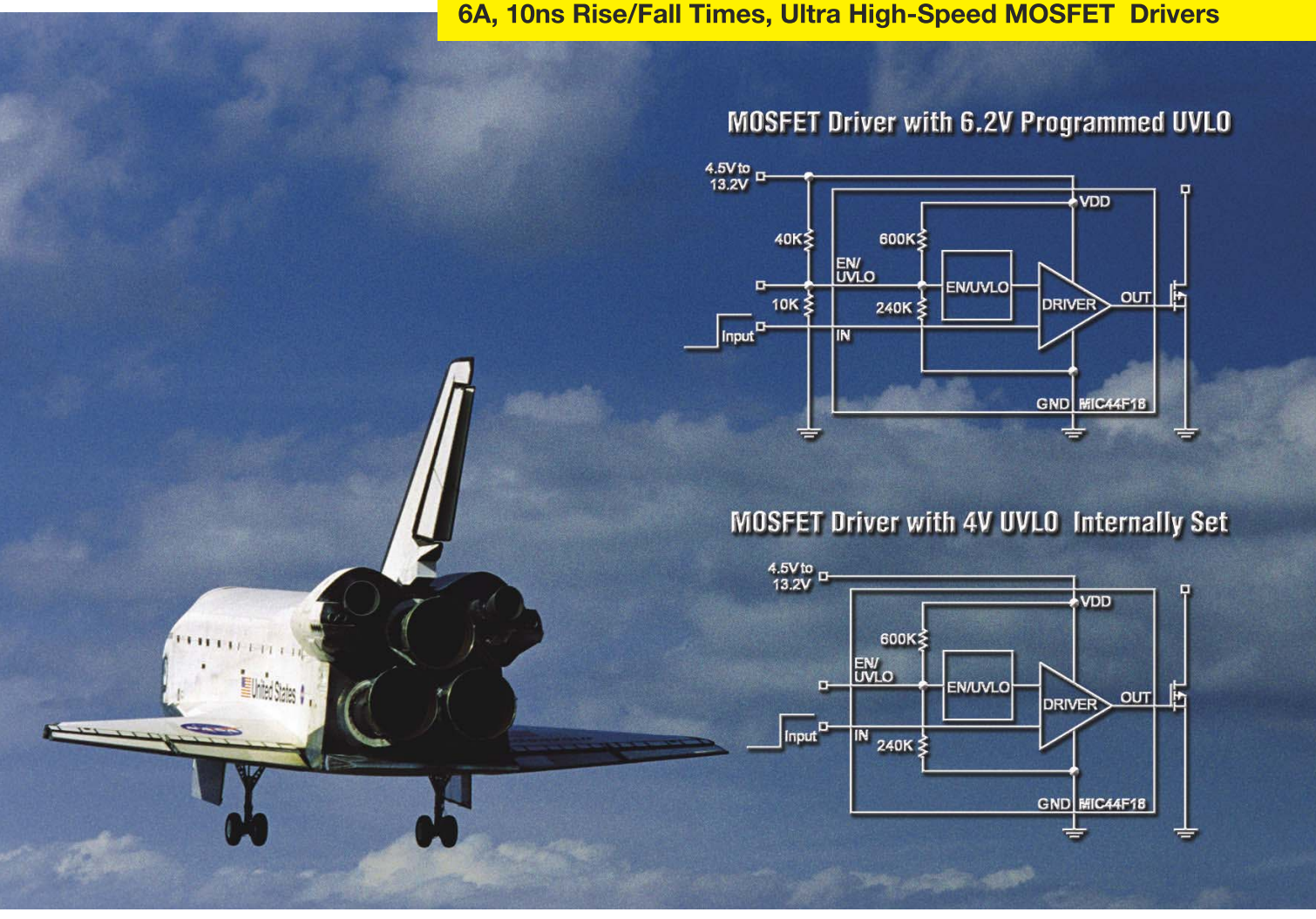

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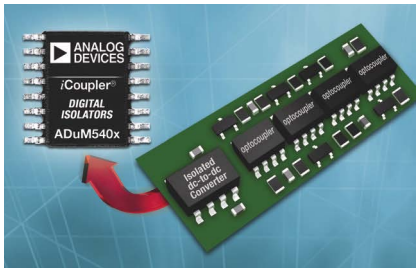
INNOVATIONS & INNOVATORS

Chip provides both signal isolation and 500 mW of regulated, isolated power

The first members of Analog Devices' isoPower family, ADuM524x, were novel in that they combined signal and power isolation on the same chip. However, the 524x products addressed only those applications needing 10 mW or less power and efficiency of only 10%. The new isoPower family members, the ADuM540x series, overcome those limitations and target mainstream applications, such as sensor interfaces. The devices up the power to 500 mW and the power efficiency to 33%. At first glance, this efficiency may seem low. However, sensors require low current levels, and most discrete dc/dc-converter ICs are less-efficient conversion components at low power levels. The company claims that, for a 20-mA current draw, the 540x requires 220 mW—less than half the 490-mW requirement for an optocoupler isolator with a discrete dc/dc converter.

The chips achieve their efficiency by using a larger iCoupler-technology planar transformer, by reducing the rectification losses, and by adding a feedback loop so that the oscillator at the transformer's input automatically adjusts to the load. The devices can provide as much as 100 mA at either 5 or 3.3V.



New members of the isoPower-chip family provide signal isolation for as many as four channels at 25 Mbps and as much as 500 mW of isolated power.

The ADuM540x family of $5 (1000), four-channel digital isolators operate at a data rate as high as 25 Mbps and come in 16-lead, wide-body SOIC packages.**—by Margery Conner**

▷**Analog Devices**, www.analog.com.

FEEDBACK LOOP

"Hold on a sec. Am I reading the article correctly? With other than a resistive (or other 'proper') load, are we actually getting more useful power than we are paying for? Is there a way to do this with gas and water also? Hey, I want to be green ... in my wallet!"

—*EDN* reader Jim in Feedback Loop at www.edn.com/article/CA6544740. Add your comments.

AMD revamps server road map

Following feedback from OEMs, microprocessor maker AMD (Advanced Micro Devices) recently updated its server road map to "strengthen its alignment with end-customer priorities" by addressing platform longevity, performance per watt, and virtualization features, according to Randy Allen, AMD's corporate vice president and general manager for servers and workstations. The new Shanghai server chip is on track to begin production in the second half of this year and will include coherent HyperTransport 3.0 for processor-to-processor communication, an increased shared Level 3 cache of 6 Mbytes instead of 2 Mbytes, and core and instruction-per-clock enhancements.

New to its server lineup is the six-core server-processor Istanbul, which will be available in the second half of 2009, aimed at allowing OEMs to preserve platform investments and increase system performance per watt. Istanbul uses AMD's direct-connect architecture, which alleviates system-communication bottlenecks. According to Allen, the company also expects in 2010 to introduce a third-generation Opteron Socket G34 platform that will contain DDR3-memory capabilities and the AMD RD890 chip set for noncoherent HyperTransport 3.0. AMD plans a six-core server process, code-named Sao Paolo, for the first half of 2010. It also will incorporate DDR3 memory and HyperTransport 3.0. A 12-core version, code-named Magny Cours, will contain the same features.

—by Ann Stefora Mutschler

▷**Advanced Micro Devices**, www.amd.com.

University working to create nanostructures to raise thin-film-solar-cell efficiency

Researchers at UCSD (University of California—San Diego) are working to create thin-film, single-junction solar cells with 45% sunlight-to-electricity-conversion efficiencies by using nanostructures that scatter and channel light. UCSD recently received a big funding boost from the US DOE (Department of Energy) Solar America program for this work.

In November 2007, Edward Yu led a team of electrical engineers who won an $885,000 grant from the US DOE to further develop their thin-film and nanowire-solar-cell devices that incorporate nanostructures, including semiconductor quantum wells and photon-scattering nanoparticles. These devices should lead to big gains in thin-film-solar-cell efficiency by increasing both the number of photons thin-film solar cells absorb and the number of excited electrons the same devices collect. According to Yu, the most recent estimate of the maximum power-conversion efficiency—under normal illumination conditions—that one can expect with this approach is approximately 45%, a large improvement over the 31% maximum theoretical efficiency for today's solar cells with classic PN junctions.

From the outside, the optimized devices behave just like traditional thin-film solar cells. On the inside, however, the nanostructures enable the solar cells to circumvent an important trade-off that has stymied past attempts to incorporate quantum wells into thin-film solar cells to boost device efficiency. Quantum wells can increase solar-cell efficiency by raising photon absorption by lowering the energy-band gap.

In the past, engineers have tried to add quantum wells to thin-film-solar-cell devices by stacking several quantum-well layers to achieve a high probability of absorption of low-energy photons. This approach, however, can be counterproductive because electron-hole pairs get stuck in the quantum wells, making it impossible for them to generate current for the device.

The UCSD engineers are using nanoparticles to scatter incoming light into paths within the quantum-well region. These paths run parallel to the PN junction, which gives photons more time to be absorbed without having to stack the quantum wells to a thickness that makes it hard for electrons and holes to escape. "Our devices have a much thinner stack of quantum wells, which means the extra photons that are absorbed are much more likely to make it out of the quantum wells and generate current. This [process] enables high photon-absorption efficiency, high electron- and hole-collection efficiency, and, therefore, also high voltage to be achieved simultaneously," says Yu.

> The UCSD engineers are using nanoparticles to scatter incoming light into paths within the quantum-well region.

Further, in this approach, the photons have a long path along the quantum wells, and the carriers have a short path to the electrode that maximizes photon absorption and minimizes a major drain on device efficiency in solar cells—electron-hole recombination. "We have already demonstrated the basic concepts in thin-film devices. I think it will take a few years to see how far this approach can be pushed to achieve really high efficiency," Yu concludes.

—by Ann Steffora Mutschler

▷**UCSD**, www.ucsd.edu.

DILBERT By Scott Adams

NASA SUPERCOMPUTER TO GET BOOST FROM INTEL, SGI

06.12.08

Intel, SGI, and the National Aeronautics and Space Administration have announced a project that aims to produce a dramatic increase in the space agency's supercomputing capacity. The Pleiades project, using SGI systems based on multicore Intel processors, will deliver a computational system with a capacity of 1 petaflops (1015 floating-point operations per second) by 2009 and then increase that figure to 10 petaflops by 2012, according to NASA. That initial milestone would represent a 16-fold improvement over the agency's current top-dog supercomputer, Columbia. That 10,240-processor system offers 88 teraflops of peak performance.

Like Columbia, the systems will reside at the NAS (NASA Advanced Supercomputing) facility. Applications will include modeling and simulations for space-vehicle design and climate modeling. "Achieving such a monumental increase in performance will help fulfill NASA's increasing need for additional computing capacity and ... the computational performance and capacity for future missions," says S Pete Worden, director of the NASA Ames Research Center.—by Matthew Miller

▶**NASA**, www.nasa.gov.
▶**Intel**, www.intel.com.
▶**SGI**, www.sgi.com.

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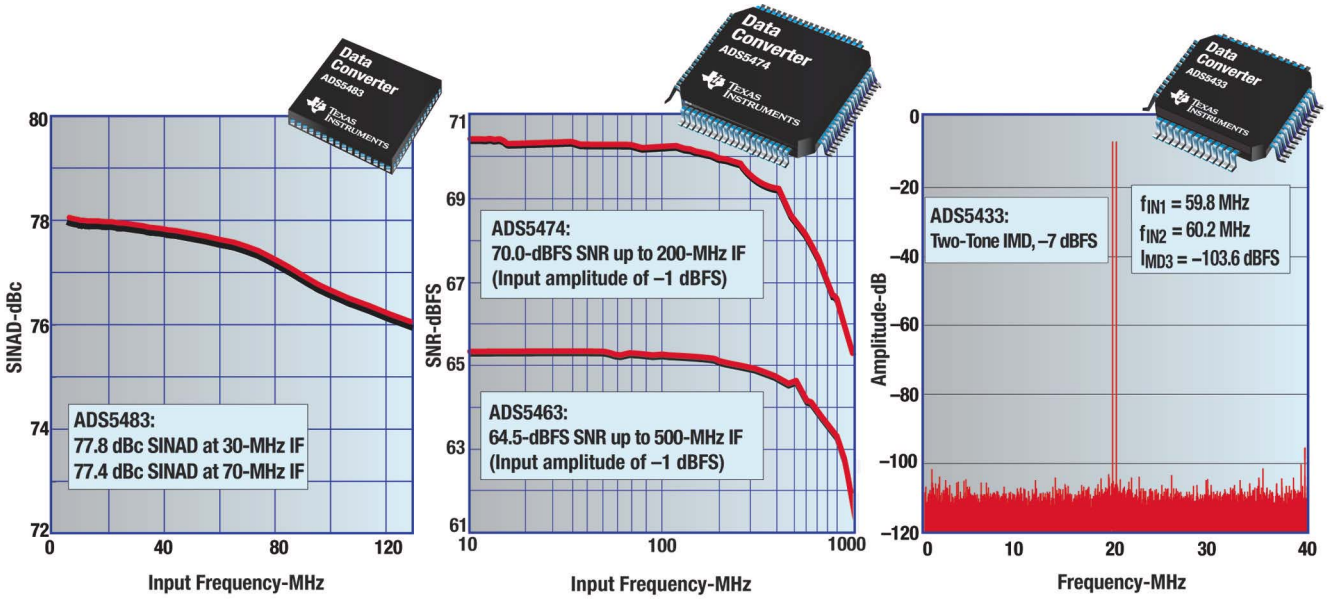

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PIC architecture supports USB across 8-, 16-, and 32-bit devices

Microchip's USB-microcontroller support now spans 8-, 16-, and 32-bit PIC devices. New USB-device families include the 8-bit PIC18F13K50 and PIC18F14K50, the 16-bit PIC24F, and the 32-bit PIC32. The free MPlab integrated development environment from Microchip supports software development for these microcontrollers and includes free USB-software stacks and USB-class drivers that developers can use with the microcontrollers. The USB-host-stack, device-stack, and class drivers are available as full source code as a download from Microchip. The embedded USB-host stack consumes approximately 25 kbytes of memory on the PIC24 and PIC32 devices when using MIPS16e instructions. When using 32-bit instructions, the embedded USB-host stack consumes approximately 35 kbytes of memory.

PIC microcontrollers support USB across the 8-, 16-, and 32-bit processor families.

Devices within each family are available for sampling now. The 8-bit PIC18F1XK50 microcontrollers include serial-communications interfaces, such as USB 2.0, I²C (interintegrated-circuit), SPI (serial-peripheral interface), and USART (universal synchronous/asynchronous receiver/transmitter). The PIC18F13K50 microcontrollers are available for $1.32 (10,000) in 20-pin SSOP, SOIC, PDIP, and 5×5-mm QFN packages; the PIC18F14K50 microcontrollers are available for $1.46 (10,000). The PIC24F USB microcontroller family supports a 2.6-µA standby current in a device that supports as much as 256 kbytes of flash and 16 kbytes of RAM. The PIC24FJ256GB1 family includes 12 devices in 64-, 80-, or 100-pin TQFP packages with prices starting at $3.47 (10,000). The PIC32 microcontroller family integrates USB 2.0 OTG (On-The-Go) support and maintains pin, peripheral, and software compatibility with Microchip's 16-bit microcontroller families. These devices support a maximum operating frequency of 80 MHz, and they include as much as 512 kbytes of flash and 32 kbytes of RAM along with the USB OTG support. The USB OTG PIC32 family member, the PIC32MX420F032H-40I/PT, is available in a 64-pin TQFP for $3.25 (10,000).

—by Robert Cravotta

▷**Microchip**, www.microchip.com.

TI ADDRESSES POWER-SUPPLY KNOWLEDGE GAP WITH PURCHASE OF REFERENCE-DESIGN COMPANY

06.12.08

The need to incorporate sophisticated power supplies into electronic systems has in recent years challenged designers. Just five years ago, digital-electronics-application designers could concentrate on their digital-hardware specialty along with the software to run it, and that focus took care of 99% of the design challenges for a new electronics product. A cheap, low-efficiency external adapter or perhaps similarly inefficient internal linear-power supply handled power. Energy was cheap, and neither consumers nor government regulators cared about wasted energy.

Those days are gone. The Energy Independence and Security Act of 2007 mandates a federal standard for external power supplies, and this year, the US Department of Energy's Energy Star label, a voluntary certification, established minimum power-efficiency and power-factor compliance for most power supplies.

Design teams must now develop design expertise in arcane specialties of power-supply efficiency and power-factor correction. Analog IC vendors, such as Maxim (www.maxim-ic.com), Power Integrations (www.powerint.com), and Linear Technology (www.linear.com), have introduced many ICs that address just these problems, but designers must select these ICs to match the application and match them with magnetics, heat sinks, and EMI (electromagnetic-interference) filters.

Texas Instruments is also addressing these problems. With its recent purchase of Commergy Technologies, a power-supply-reference-design company, TI is recognizing that its value added in the power-supply market must address the knowledge gap in the electronics-design world. Commergy's expertise in creating these reference designs includes planar magnetics, power-factor correction, power-topology design, thermal management, and EMC (electromagnetic-compatibility) design. In short, TI has purchased an integrated outsourcing path for its customers' power-subsystem designs.—by Margery Conner

▶**Texas Instruments, www.ti.com.**

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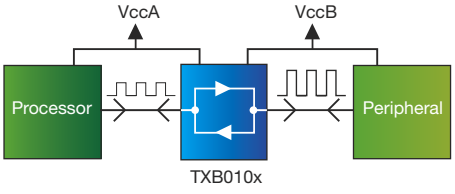
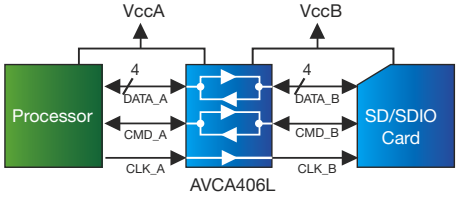


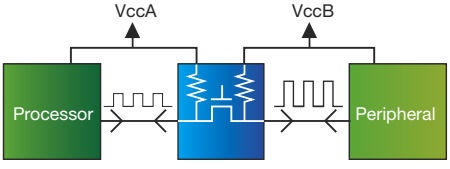
TXB010x

Application-Specific Translators (Memory Card Interface)



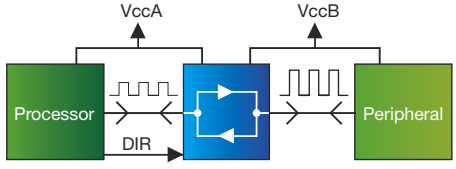
AVCA406L

Auto-Direction-Sensing Translators for Open-Drain Applications



TXS010x/E

Dual-Supply-Configurable Translators



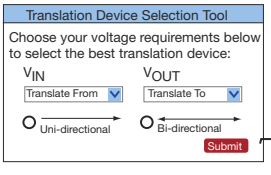
AVCxT245

TI Has the Translation Device for You.

Texas Instruments offers a wide-ranging selection of voltage-level translation devices from auto-direction-sensing and dual-supply-configurable devices to application-specific memory card interface translators. When mixed-voltage issues become a concern in your design, TI has the translation device that fits your requirements.

Device	Bit Width	VccA (V)	VccB (V)	ESD Protection	Smallest Package
Auto-Direction Sensing Translators*					
TXS0102	2	1.2 to 3.6	1.65 to 5.5	8-kV HBM	8-bump WCSP
TXS0104E	4	1.2 to 3.6	1.65 to 5.5	15-kV HBM	12-bump WCSP
TXB0104	4	1.2 to 3.6	1.65 to 5.5	15-kV HBM	12-bump WCSP
TXB0108	8	1.2 to 3.6	1.65 to 5.5	15-kV HBM	20-ball BGA
Application-Specific Translators (Memory Card Interface)					
AVCA406		1.4 to 3.6	1.4 to 3.6	15-kV Air Gap Discharge (IEC)	48-ball VFBGA
AVCA406E		1.2 to 3.6	1.2 to 3.6	15-kV Air Gap Discharge (IEC)	20-ball VFBGA
AVCA406L		1.2 to 3.6	1.2 to 3.6	6-kV HBM	20-ball VFBGA
CF4320H		1.65 to 3.3	3.6 to 5.5	15-kV HBM	114-ball LFBGA
Dual-Supply Configurable Translators*†					
SN74AVC1T45	1	1.2 to 3.6	1.2 to 3.6	2-kV HBM	6-bump WCSP
SN74AVC2T45	2	1.2 to 3.6	1.2 to 3.6	8-kV HBM	8-bump WCSP
SN74AVC8T245	8	1.2 to 3.6	1.2 to 3.6	8-kV HBM	24-pin QFN
SN74AVC16T245	16	1.2 to 3.6	1.2 to 3.6	8-kV HBM	56-ball VFBGA
SN74AVC32T245	32	1.2 to 3.6	1.2 to 3.6	8-kV HBM	96-ball LFBGA

** Other bit-width options available. † Bus Hold feature available.*



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Finding the right Translation Solution is Easy with TI's Translation Selection Tool

TEXAS INSTRUMENTS

Power-management IC integrates seven programmable regulators

Summit Microelectronics' new SMB119 power-management IC provides all the power rails needed for a modern handheld product. The part integrates three synchronous buck regulators, two boost converters, one configurable buck-boost converter, and one low-dropout linear regulator. Input voltage is 2.7 to 6V. The device can operate at 95% efficiency and has a standby current of 0.1 µA.

The switching regulators have a PWM (pulse-width-modulation)-override mode to reduce EMI (electromagnetic interference). The IC also provides power supervision to monitor overvoltage or undervoltage conditions. It communicates with the system processor over an SMB (system-management bus) or an I²C (interintegrated-circuit) bus. The SMB119 targets applications in portable consumer electronics, such as digital still cameras, digital camcorders, MP3 and MPEG-4 portable media players, GPS (global-positioning-system) terminals, portable medical equipment, personal digital assistants, and the next generation of mobile smartphones.

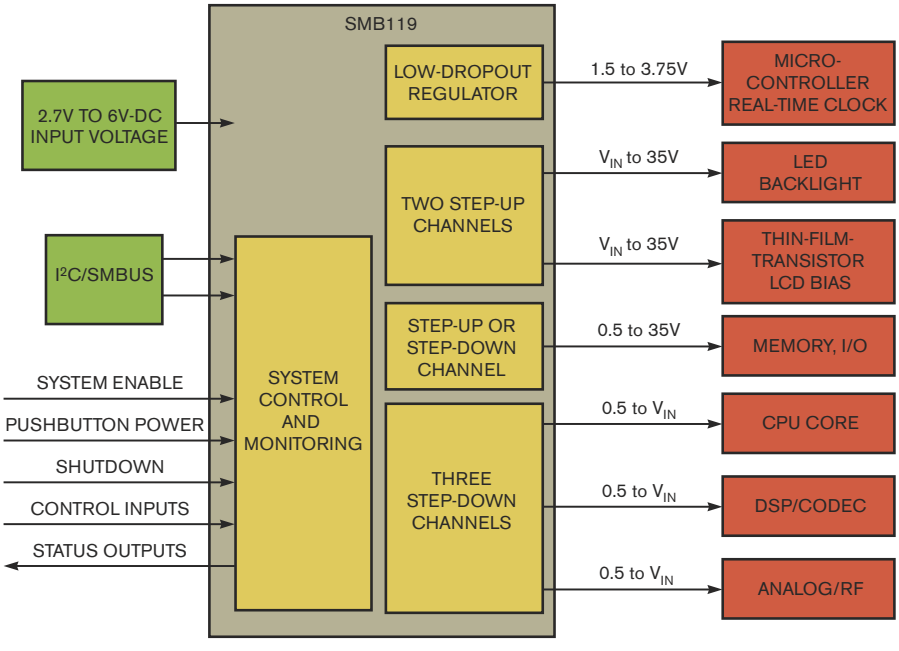
The evaluation board works through a USB port with Summit's Windows-based GUI (graphical user interface) that allows designers to set up regulators and supervision parameters and then program them into nonvolatile memory. Once designers define the part's functions, they can extract a hex file from the evaluation board that will allow Summit to provide the part in volume quantities. You can download the design-kit software from Summit's Web site.

The device comes in a 0 to 70°C or −40 to +85°C operating range and in a 7×7-mm, 48-pad QFN package with a suggested retail price of $3.74 (10,000). Samples and evaluation modules are available. Volume production has just begun. An available reference design incorporates the SMB119 along with an SMB137 switch-mode charger.

> A Windows-based GUI allows designers to set up regulators and then program them into nonvolatile memory.

—by Paul Rako

▷**Summit Microelectronics**, www.summitmicro.com.



The SMB119 power-management IC provides handheld-product designers seven voltage regulators as well as supervisory functions.

LOW-POWER ENVIRONMENT TARGETS CHIP DESIGN

06.12.08

Further backing its support for the UPF (Unified Power Format) for exchange of power-related design data between EDA-chip-design tools, Synopsys has assembled a comprehensive array of tools for achieving power-related design objectives. The Eclypse tools span system-level, verification, implementation, sign-off, and IP (intellectual-property) methodologies and services for low-power-chip development.

Synopsys will host a series of low-power-design seminars as part of its promotion of the concept. Using the tools, the company says, you will be able to apply techniques such as multithreshold-CMOS-power gating and multivoltage and dynamic-voltage and frequency scaling in a less time-consuming manner, requiring less manual verification.

The company based the suite on the *Low-Power Design Methodology Manual*, which Synopsys and ARM (www.arm.com) co-authored; the approach also extends to the Innovator environment for embedded-software design. In that context, you can run software on a virtual platform using fast models of processors and IP blocks.

—by Graham Prophet

▶**Synopsys, www.synopsys.com.**

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Synopsys' Aart de Geus on investing to win

Aart de Geus, PhD, is chairman and chief executive officer of semiconductor-design and -manufacturing-software supplier Synopsys. He helped invent the Design Complier software tool and is a fellow at the IEEE.

What are the biggest challenges that your customers want you to solve?

A I like to use the term 'techonomics' because there are technical challenges, and there are economic challenges, but they are on an intersection, which is: You can solve anything if you have infinite money, and, obviously, you don't. Our customers are rethinking everything they do right now around the notion of critical mass, which is not infinite money, but sufficient money to solve the problems, including doing it with others. You want new technologies, you can't afford it yourself, and [determining] who to team up with is a good example. You have issues in getting your design flow to end up with chips on schedule, so you'd better team up with somebody really proficient in the EDA category because all of these things interact.

Also, the gluing together of Frankenstein flows is [not working]. Frankenstein has run out of runway! More independent, best-in-class tools give worst-in-class results. These [approaches] are all forms of establishing critical mass around your issue. If you look at what the issues are on the design, it is very, very clear that two or three stand out. One is the pairing of timing and power. Power is such a dominant issue, and there are some very cool escape values in terms of new architectures. But, fundamentally, it is a center of gravity. The second one is clearly everything that touches the word 'verification' because the verification problem is growing much more rapidly than Moore's Law for a variety of reasons. By the way, in verification, you have to throw in the embedded software because, ultimately, you have to understand about the physical aspects.

On the economic side, it is so much a market of 'winner takes all.' Therefore, if you're not on a big win, do you really want to continue? You may be better off searching for the next big win.

How is multicore impacting what customers want?

A There are two very different angles to that [question]. One is multicore as a thing that influences how we write our software versus multicore as what are the things [we need to do] in design. In the first case, last year, we delivered quite a number of tools that are multicore/multithread, and some problems are better suited to split up. But, in general, there's no question

that there will be more computation capabilities on a variety of multicore [products]—not necessarily heterogeneous ones—and that [trend] will continue. There will be all kinds of transition questions … and the transition may not be as fast as the capability, but we are utterly on top of it. We have a center of excellence within Synopsys dedicated to multi-fill-in-the blank techniques that helps all of our projects take advantage of this [ability]. We are engaged with the people providing the processors—Intel, AMD, or Nvidia—on what is coming.

On the other side, our insight into people designing these things clearly is a whole new world that is appearing on one hand, but it's not coming from the silicon side. The silicon side is just more of the same; it's just a different architecture. It's got to be on the embedded software, so I'm very interested in what that [software] is and the verification that is related to that.

Is the economic slowdown impacting Synopsys?

A It's not an issue for us. But I do think it is an issue for a number of people because, whenever you have slowdowns or phase shifts in a market, it invariably means there are winners and losers. We've been predicting this [scenario] for quite a while on the very simple basis that, if you look at the economics of what's happening in semiconductors, they have grown nonlinearly, and that [growth] means that the price to play is substantial. For example, if you want to develop the next technology node, a billion dollars is a good starting point. If you want to have a fab, $3 billion is a good starting point. If you want to build a chip, $10 million is a good starting point. You use those numbers, and you immediately conclude that not everybody can play. Now, that doesn't mean that there won't be a lot of economic activity; it means that the activity changes because, 'hey, why don't you and I share a fab?' That's called a foundry in some ways. Why don't I, instead of using five suppliers of something, get a much closer relationship with one that can then grow and give me better results than my gluing it all together. When there is stress on a system, not everybody walks out equally happy, so the key is: Did one prepare and invest in the right aspects to be a winner under stress?

What is your plan for investing to win?

A We've invested for a number of years based on five tenets. The first is: Best-in-class products are necessary. Second, you need to have a complete offering because people are going to fewer suppliers. Third, the product needs to be integrated because products are no longer independent. The fourth tenet is 'roots down' because, with smaller geometries, the amount of physical issues bubbling up through design for manufacture is huge. And the fifth tenet is 'reach up' because more [functions are] embedded software, embedded intellectual-property blocks, and so forth.

—by Ann Steffora Mutschler

RAQ's

Rarely Asked Questions

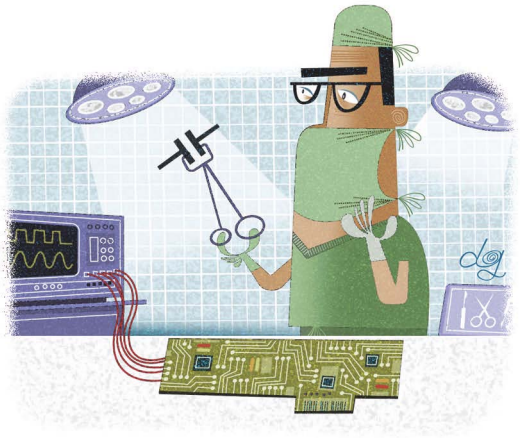
Strange stories from the call logs of Analog Devices

Contributing Writer John Ardizzoni is an Application Engineer at Analog Devices in the High Speed Linear group. John has been with Analog Devices since 2002, he received his BSEE from Merrimack College in N. Andover, MA and has over 28 years experience in the electronics industry.

A Capaciticectomy? Sounds Awfully Painful!

Q. One of your high-speed triple amplifiers is oscillating. What's wrong with it?

A. Well there are a variety of things that could be wrong with the "circuits," but most likely there nothing intrinsically wrong with the amplifier. With many high-performance amplifiers, however, you do need to pay close attention to layout and bypassing. If ignored, you and your circuit could feel a little ill.



With wideband devices, you need to be careful and pay attention to the small details. In this case, it turned out that the oscillation experienced by the customer wasn't caused by the amplifier itself, but by poor layout.

To be specific, the problem was parasitic capacitance at the inverting input of the amplifier to ground. Capacitance at the inverting input introduces a pole in the amplifier's loop response, lowering the amplifier's phase margin and causing instability, peaking, and ringing. It doesn't take much capacitance[1] to cause an oscillation, and you can easily accumulate 2 to 3 pF of capacitance at the summing node (inverting input) if you're not paying attention to layout. I always advise customers to breadboard the circuit if possible, and to test the heck out it in the lab. A high-performance simulated design can be rendered useless if proper layout guidelines are not followed.

The solution is a capaciticectomy (not really a word) — although it's quite difficult to remove parasitic capacitance after it has infiltrated your board. Therefore, in these cases, prevention is the best medicine. The capacitance is formed by the small mounting pads of the amplifier, gain setting and feedback resistor pads, board dielectric and the ground plane. We always recommend removing the ground plane from beneath the amplifier mounting pads and around the summing node where the feedback and gain set resistor pads are located. Doing so effectively removes the bottom plate of the parasitic capacitor and therefore eliminates the capacitance. This applies equally to the output, as parasitic capacitance at the output can also cause similar problems.

As with humans, a little preventative medicine goes a long way. Paying attention to board layout issues at the onset of your design, will keep you and your circuit in tip-top shape!

Keep an eye out for our New and Improved webinar this October, "A Practical Guide to High-Speed Printed-Circuit-Board Layout."

[1] *Some customers ask how much capacitance is enough to cause a circuit to oscillate. I sometimes tell them a 1000pF is enough. Confused looks abound and I explain to them that if 1pF = a puff, then a 1000pF = 1 nF, then it stands to reason 1 nF = a nuff and a nuff is enough!*

To Learn More About Board Layout

Go to: http://rbi.ims.ca/5713-101

Have a question involving a perplexing or unusual analog problem? Submit your question to: raq@reedbusiness.com

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BY BONNIE BAKER

Analog filter eases delta-sigma-converter design

Delta-sigma converters with sinc (sinx/x) digital filters change the signal chain's complex antialiasing-filter requirements to a simple, first-order, passive filter. With this "easy-to-design" circuit, you can tackle the major noise contributors around the delta-sigma modulator's sampling frequency. The converter's characteristics that you use in this filter design are the modulator-sampling rate, F_S, and output-data rate, F_D.

The frequency response of a sinc digital filter looks like a comb (**Figure 1**). The frequency of the first null in this **figure** is equal to the F_D of the converter. If you look at the frequency response of a sinc filter up to the modulator's sampling rate, you can see that the sampling frequency is much faster than the converter's output-data rate.

Because a delta-sigma converter is a sampling system, all noise and signals above one-half of the F_S alias back. The sinc digital filter rejects noise over a wide frequency band, but it does not reject system noise around the F_S. The amplitude of the noise and signals hovering around the sampling frequency is small, but noise is a reality. The lower bits may fluctuate because you have a high-resolution converter.

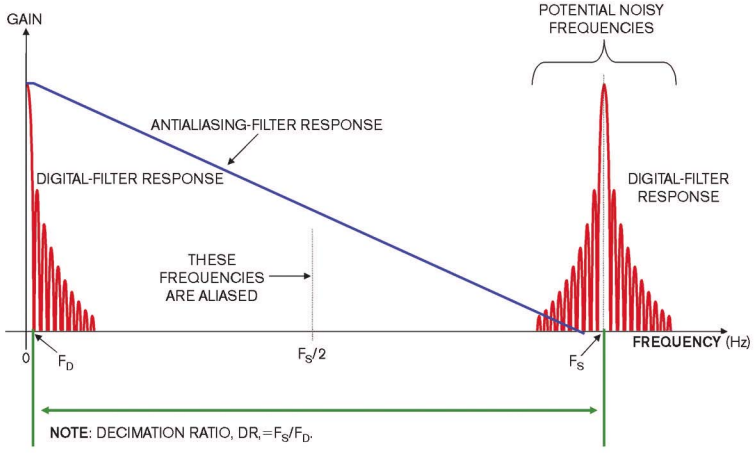

Figure 1 The sinc-digital-filter response is compressed near 0 Hz, and the converter's sampling frequency mirrors and duplicates that response.

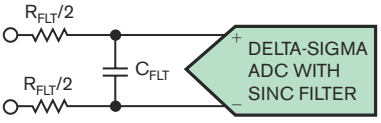

Figure 2 This filter has two equivalent resistors and a capacitor.

The corner frequency of your analog filter is equal to the output-data rate, or F_D. Fortunately, this filter has a low-order function, and the appropriate choice is a simple RC filter. If your system has a lot of noise or signals around the region of F_S or if the decimation ratio is less than 100, consider using a second-order, lowpass filter.

Place the analog antialiasing filter before the input of the converter. **Figure 2** shows the best option for this passive, lowpass filter for a single-channel device, where $F_D=1/(2\pi R_{FLT}\times C_{FLT})$. Because the lowpass filter is a simple RC pair, the values of the filter's resistors ($R_{FLT}/2$) are easy to choose as long as the resistor noise from dc to the filter's corner frequency is less than one-third of the noise that the delta-sigma converter generates. The value of the capacitor (C_{FLT}) should be at least 20 times higher than the input capacitance of the converter. It can be as high as you want, as long as you keep in mind that your filter's corner frequency is equal to or greater than the converter's output-data rate.

If you have extraneous noise in your system, you will be pleased with the results of using this antialiasing filter. You may not find noise in your lab conversions, but make sure you anticipate the location of your system. In the field, extraneous and noisy signals may very well just creep into your converter. EDN

Bonnie Baker is a senior applications engineer at Texas Instruments and author of A Baker's Dozen: Real Analog Solutions for Digital Designers. *You can reach her at bonnie@ti.com.*

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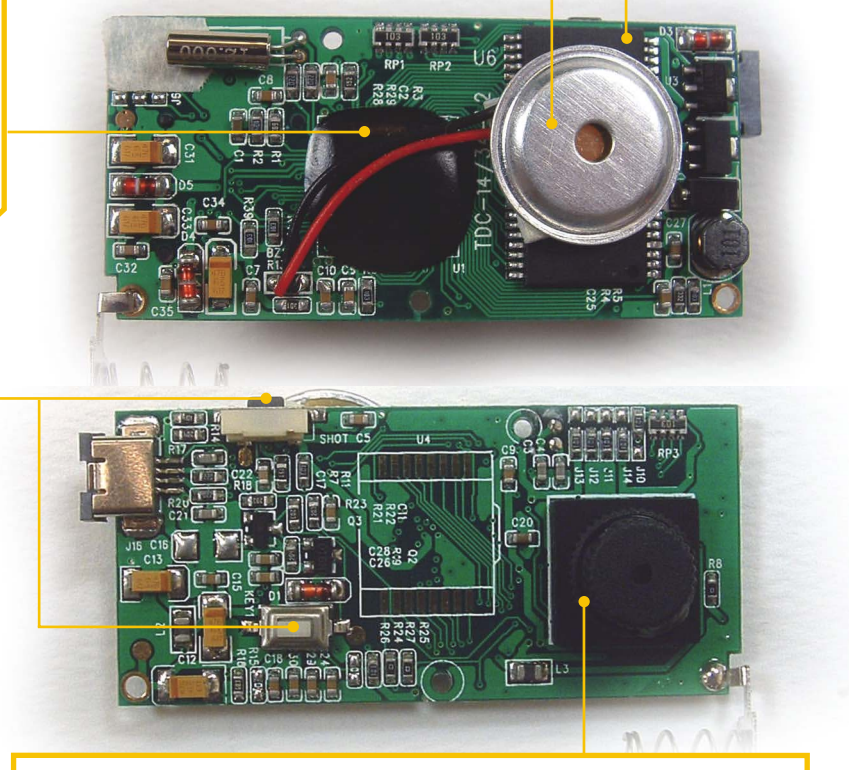
Low-cost snapshots: dismembering a diminutive digicam

PRYING EYES QUERIES THE CONTENTS OF A SUB-$10 KEYCHAIN CAMERA

Prompted by a tempting ink-jet-printer-rebate promotion, I this year purchased Argus' bundled $9.99 DCM-099 0.3M-pixel digital camera with a "Prying Eyes" analysis in mind. What's inside the unit's petite silver-plastic case, and do its picture-taking abilities belie my price-defined modest expectations?

A simple piezoelectric speaker beeps to alert the user of camera power-on and -off and mode transitions, along with image-capture completion. Underneath it is what I first assumed to be a 2-Mbyte NAND-flash-memory chip. The item's ESMT M12L616A part number, however, told me I had a 16-Mbit SDRAM on my hands. Don't remove the single AAA battery or allow it to drain before PC transfer, or you'll lose your stored pictures!

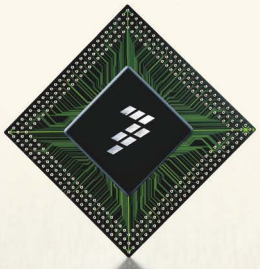
The lack of any visible memory IC save the PSOP (power-small-outline-package)-encapsulated SDRAM suggests that system code resides on the same slivers of silicon that implement the camera's "brains." Speaking of encapsulation, you'll likely find the chip's onboard system processor under the blob of black epoxy in the center of the PCB (printed-circuit board). Its specifics are unknown.



Two membrane switches—one to activate the shutter, and the other for mode toggling and selection—implement the entirety of user input. User feedback, such as remaining-picture count, relies on a low-resolution monochrome LCD, connected to the PCB via zebra-strip elastomers.

This design perfectly exemplifies Moore's Law's strengths and limitations. The amount of double-sided PCB surface area that digital-logic and memory circuits, including their large packages, consume is only around 20% of the total available real estate. Conversely, discrete capacitors, diodes, inductors, resistors, and resistor packs, along with a few power transistors, dominate the topology.

A lens labeled as having a F2.6 fixed aperture and 5.4-mm fixed focal length, along with fixed focus, handles incoming photon collection. Underneath it is a VGA-resolution, 640×480-pixel sensor, which I strongly suspect Argus' supplier implemented in CMOS and which I also strongly suspect contains the intelligence necessary to tackle JPEG conversion and other image-processing functions. The DCM-099 captures still pictures in both high and low resolutions and at two quality-versus-size compression-ratio options, translating to peak resident storage of 26 to 208 images. It even supports the capture of 6-frame/sec AVI video streams.



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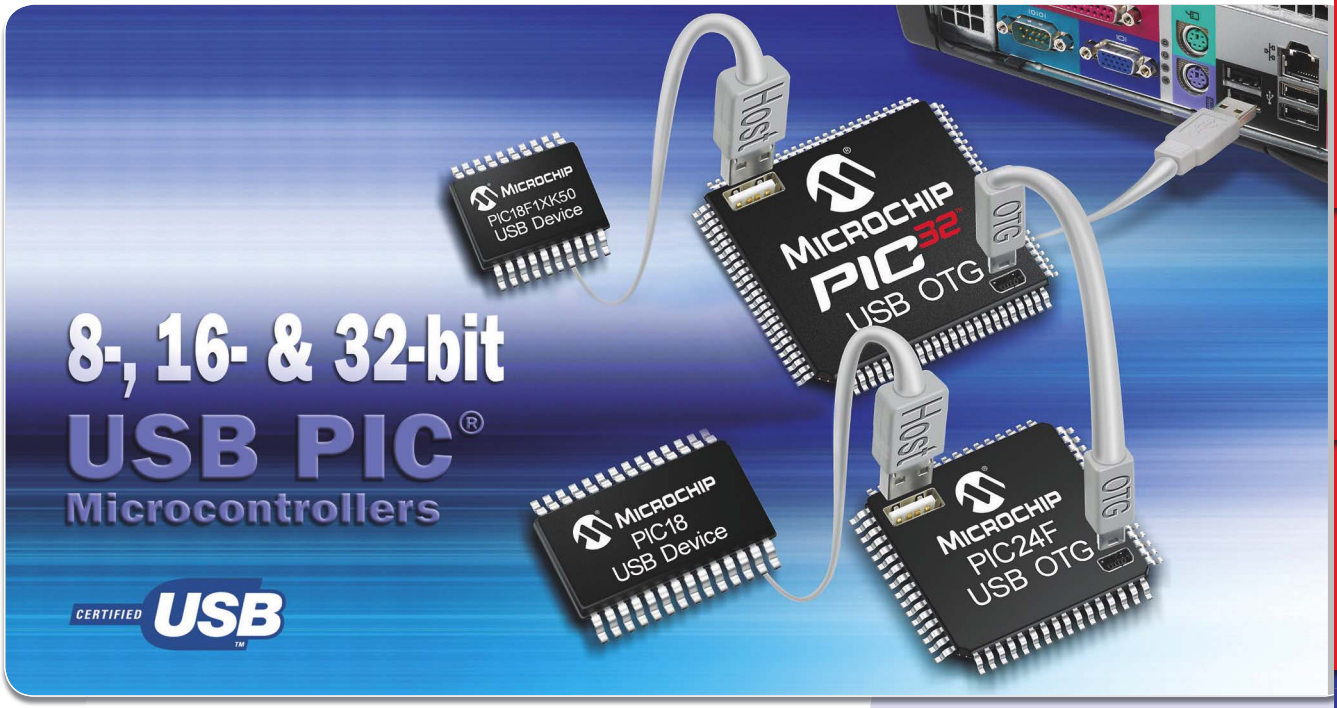

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MICROCHIP

BY PAUL RAKO • TECHNICAL EDITOR

PAY CAREFUL ATTENTION TO ANALOG SWITCHES AND MULTIPLEXERS, WHICH ARE CRITICAL COMPONENTS OF THE SIGNAL PATH. DESIGNERS SHOULD UNDERSTAND THE APPLICATIONS AND SPECIFICATIONS OF THESE IMPORTANT ANALOG PARTS.

USE ANALOG SWITCHES TO MULTIPLEX YOUR SIGNALS

Few IC-schematic symbols are simpler than the one that depicts an analog switch (**Figure 1a**). A basic switch comprises just an input, an output, a control pin, and a couple of power-supply pins. Yet, bedazzling complexity hides behind this simple appearance (**Figure 1b**). Several specifications, including power-supply voltage and on-resistance, are fundamental to the part's operation. An analog switch also has many ac specs, such as bandwidth and switching time. All these specs, including leakage current, change—sometimes radically—over temperature. As with all other analog parts, the switch has specs that all interact and lie along a continuum of values. These specs are not black and white, just shades of gray (**Reference 1**).

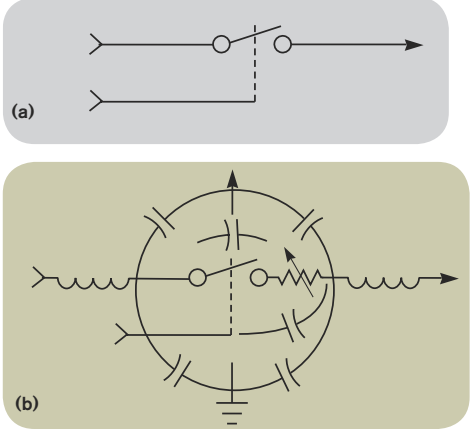

Figure 1 A simple symbol represents an analog switch, but stray capacitances abound and small inductances occur because of the presence of bond wires (a). The on-resistance is variable with applied signal and power supply, and the capacitors also change with applied voltage (b).

One analog switch is complex, but groups of them that you gang together or integrate into one IC to provide DPDT (double-pole/double-throw) functions or multiplexers are even more complex. For example, a multiplexer that feeds signals to an ADC should be a break-before-make device—that is, it should break contact before it makes contact, keeping the input signals from short-circuiting each other. But a multiplexer on an audio output may need to be a make-before-break device—that is, it must make contact before it breaks contact to prevent objectionable clicks or pops in the audio signal. As with all analog parts, things are more complicated than they seem at first glance.

FINDING NEW USES

Analog switches have always had a place in instrumentation and industrial markets. Data-acquisition cards reroute the analog inputs to provide many channels of measurement that travel to an ADC, and they route analog outputs to connectors or internal circuit nodes. The analog switches and multiplexers in these cards have traditionally been high-voltage parts, in keeping with their industrial, military, and medical heritage. These decades-old applications will always be with us, but several new technological developments are making dramatic use of analog switches.

One of the highest volume uses of analog switches is in cell phones and other handheld consumer devices. "I don't

know of a cell phone that does not have at least one switch in it," says Jerry Johnston, Fairchild Semiconductor's product-line director for switch products. Size and features are the driving factors in the use of analog switches in phones. Phone cases have little room for connectors, meaning that analog switches must route signals from multiple ICs to one USB port, video port, audio port, or power connector. These switches also have a plethora of features, further increasing their use in cell phones. A basic cell phone typically comprises a baseband IC and the RF-signal chain. A full-featured phone may also include a digital camera and a videocamera, both with associated flash systems, and can serve as an MP3 and video player. It also provides for USB, Bluetooth, and wireless-LAN connectivity. Johnston knows of some high-end cell phones with as many as 14 analog switches.

For similar reasons, another growing application for analog switches is in laptop computers. Even bare-bones laptops have cameras, IR (infrared) ports, Bluetooth, and wireless functions. Also similar to cell phones, laptop computers have a limited amount of outside surface on which to put connectors. Although less severe than the space restrictions for cell phones, this limitation still provides many applications for analog switches.

Home entertainment is another high-volume application for analog switches. Anyone who has had to hook up a TV, a DVD player, a stereo receiver, a gaming system, a cable system, and a computer can attest to the video- and audio-signal-routing challenges that these tasks entail. As with cell phones, these home-entertainment systems may use some digital signals, but you still must use analog switches to route this equipment. For example, many home-entertainment systems have multiple HDMI (high-definition-multimedia-interface) digital-signal paths, and these products need analog switches to route those signals because using digital switches can cause skew and delay. A digital switch creates one or more gate delays as it functions, and those delays may be nondeterministic, instead changing with switch routing or temperature, and the gates' rise and fall times may change the duty cycle of the digital signal.

Yet another high-volume application of analog switches is automotive entertainment, which has all the same signal-routing problems as, but with less space than, a home-entertainment system. Automotive electronics, or "telematics," combine the signal-routing and management challenges of the entertainment, computer, and cell-phone environments.

AT A GLANCE

- The key specs for analog switches are voltage, on-resistance, capacitance, charge injection, speed, and package.
- Dielectrically isolated processes prevent latch-up in some switches.
- Switches can work from dc to 400 MHz and beyond.
- MEMS (microelectromechanical-system) switches work well at high frequencies but have reliability problems and expensive packaging.
- Be sure to model all the parasitic elements if you are simulating an analog switch.

IMPORTANT SPECS

How much voltage an analog switch can withstand is just as critical as the voltage rating on a mechanical switch, sometimes indicating the switch's intended market. Switches with voltages of 12 to 36V often target the instrumentation, military, and medical markets. Data-acquisition systems that must measure some unknown voltages from the outside world also benefit from using analog switches with high voltage ratings. Because designers have no control over the level of the measured voltages, it is important for the switch to be able to handle as much voltage as possible. It is this same quest for robustness that led to the development of dielectrically isolated and fault-protected analog switches.

Dielectric isolation puts each transistor in the IC in its own glass enclosure (**Figure 2** and **Reference 2**). Glass has a lower dielectric constant than silicon, yielding very low internal capacitance for dielectrically isolated parts. As a result, the formation of a parasitic SCR (silicon-controlled rectifier) can cause latch-up in the IC substrates if an input signal goes outside the power-supply rails (**Figure 3**). Manufacturers typically fabricate parts for consumer electronics on inexpensive CMOS process, and these parts have maximum voltage ratings of 5.5V. For example, Fairchild's FSA2270T dual-SPDT (single-pole/double-throw) analog switch swings below the negative rail so that it can pass bipolar-audio signals when it has no negative-power-supply rail (**Reference 3**). Another example, Texas Instruments' TS3USB221 multiplexer/demultiplexer switch, operates from a 2.3V supply.

Fault protection is another important spec. Devices with this feature incur no damage even if the input-voltage exceeds the power-supply rails. The Maxim MAX388 analog multiplexer, for example, has fault protection to 100V. In addition to providing internal fault protection, your circuit can be designed to protect analog switches for overvoltage conditions (**Reference 4**).

On-resistance is another vital spec of an analog switch. On-resistance may seem unimportant if your design includes an operational amplifier that provides buffering to the analog switch. The op amp's input impedance may be in the megohms, so putting a 100Ω

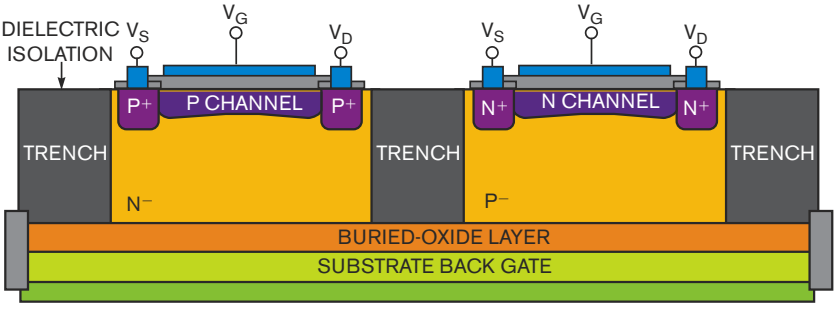

Figure 2 The dielectrically isolated process isolates each transistor in an IC with an oxide trench. This approach prevents latch-up and lowers stray capacitance (courtesy Analog Devices).

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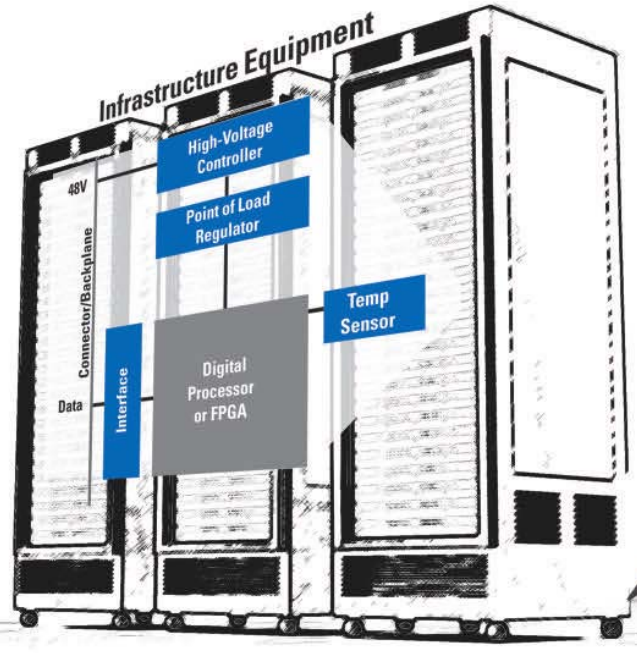

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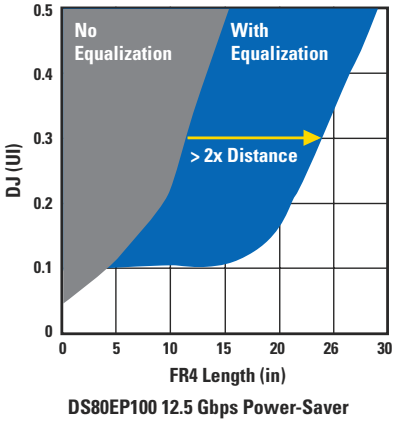

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analog switch in series with the input means that this impedance is negligible, but only at dc. The on-resistance of the switch can react to the stray capacitance and input capacitance of the amplifier. This reaction can create a pole that rolls off the frequency response of the signal chain, perhaps to unacceptable levels. Many other signal-routing applications need far lower on-resistance. Whereas 100Ω was acceptable decades ago when engineers used Fairchild's ubiquitous CD4066 CMOS analog switch, many devices' on-resistances soon decreased to 10Ω, and several less-than-1Ω analog switches are now available. For example, the Pericom PI3A3159 SPDT analog switch has an on-resistance of 0.4Ω. These new parts reach low on-resistances at operating voltages as low as 2.7V.

Another specification of importance, off-resistance, measures the switch's ability to block a signal. The fundamental off-resistance of an analog switch is the off-resistance of a MOS transistor, which is usually higher than most circuits need. The off-resistance is also a function of the ESD (electrostatic-discharge)-protection diodes that are on the IC die to prevent damage in handling and assembly of the transistors (**Figure 4**). It may help to think of off-resistance as a leakage specification. Because leakage doubles with every 10°C, you should always check the off-resistance at the maximum temperature at which you expect your circuit to operate. Also, off-resistance and leakage are specifications that apply at dc or low frequencies. At higher frequencies, switch capacitance dominates off-resistance and leakage.

Capacitance is unavoidable in anything as small as a modern analog switch. The pins are close together, so you can expect a few picofarads of coupling between them. You must also contend with the capacitance between the transistor structures and the substrate. Manufacturers fabricate modern parts on proprietary processes so that the parts can operate into the RF range—easily hundreds of megahertz. Some customers ask manufacturers to specify analog switches with insertion and return losses, specs associated with RF design, according to Manav Malhotra, an associate business manager at Maxim Integrated Products. Semiconductor analog switches also have an Achilles' heel:

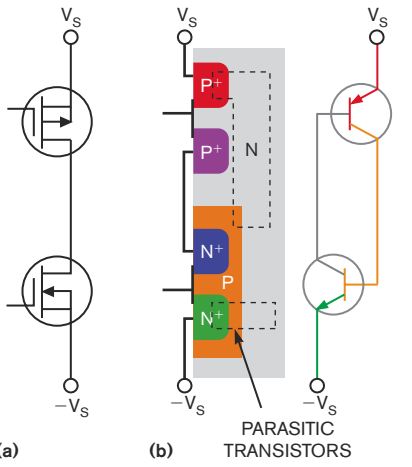

Figure 3 Chip designers use P- and N-channel FETs in CMOS ICs (a). When the inputs to the transistor exceed the power-supply rails, latch-up conditions occur. This excursion causes free carriers in the substrate, which triggers the creation of a parasitic silicon-controlled rectifier (b). This excursion also shorts the positive-supply voltage to the negative-supply voltage.

the capacitance between various pins and to ground or power. Reed relays and MEMS (microelectromechanical-system) switches have smaller stray capacitance, making them suitable for frequencies well into the gigahertz range, but both relays and MEMS are mechanical devices and will wear out with hundreds of thousands to millions of cycles. Reed-relay switches also need a lot of power to actuate, and MEMS devices require expensive packaging to keep the silicon beam in a hollow area so that it can operate. Even if your signals are only hundreds of kilohertz, you should look at the analog switch's capacitance between pins, including ground and power, to decide whether the part will provide the needed isolation and crosstalk specifications.

Charge injection is another important specification in analog switches. Turning on a switch tends to inject charge into the signal path, which can be catastrophic in sample-and-hold regulators and in multiplexers that feed an amplifier. IC designs that match internal capacitance inside the part can minimize charge injection. The faster the rising edge on the actuating signal, the more of a problem that charge injection will be. Lowering the slew rate of the analog-switch control signal may reduce the charge injection to acceptable levels. Be sure to evaluate this factor if your design has any high-impedance nodes in the signal path. Charge injection is often a cause of pops and clicks in audio circuits that incorporate analog switches. As with all specs, check this factor over the temperature at which you expect your design to operate.

Many analog switches route fast digital signals, so the speed of actuation is an important spec for many users. Even in legacy applications, such as data-acquisition multiplexers, you must factor in the speed of the switch to the sample-and-hold analysis to ensure that the signal has settled to an accurate level before the ADC measures it. You should also note the PSRR (power-supply-rejection ratio) of any analog switches in a signal chain. Just as the capacitance between outputs and power can attenuate a fast signal, that same capacitance can pass a high-frequency noise component on the power rail into your output signal. These days, switching power supplies power many analog circuits. Be sure to examine the spectral content of the power rail. If frequencies are high enough, they will pass into your design's output through the internal capacitance in the analog switch. Placing a resistor or an inductor in series to the power-supply pin of the part and one or more decoupling capacitors close to the analog switch ensures that noise from the power supply does not enter your design's signal path. It will also make the circuit more immune to RFI (radio-frequency interference, **Reference 5**).

A spec that may be as important as any other is the package the part comes in. If you are designing a handheld instrument or a cell phone, you need your device to fit into an SC-70 or a smaller package. If you are using the part to switch power, then you may want a large package to aid in the power dissipation to keep the part from becoming too hot. Another package consideration is conformance with a standard part's pinout. If you need to upgrade an Intersil DG403 monolithic analog switch, for example, then you need a part that uses an identical package and pinout. Getting a part with low on-resistance in a small package is a challenge. "The challenge with most switches is physics," says Jeffery

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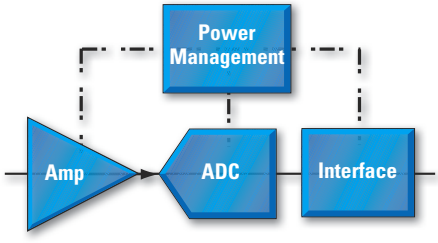

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DeAngelis, executive director of the interface-switch-and-protection-business unit at Maxim Integrated Products. "To get a smaller on-resistance, you parallel multiple fingers [gate structures] in your FET. When you do that, you get lower on-resistance, but the die grows."

Current consumption is yet another critical parameter. Some parts change supply current depending on the level of the control signal you apply to them. Evaluate supply current on a breadboard; don't assume that the nominal figure on the data sheet applies to your circuit. Also be aware that the supply current changes over temperature.

HANDLING TRADE-OFFS

With so many specs to consider, it would behoove a diligent analog engineer to examine the basic trade-offs inherent in analog switches. All engineers know that the most important spec is price. For a low-cost switch, you can't beat an old CD4066 CMOS analog switch. It works at voltages as high as 15V, and you can use more than one switch in parallel to achieve a reasonable level of on-resistance. At the other end of the spectrum, the dielectrically isolated Intersil HS-303ARH has a radiation-hardened silicon gate that makes it suitable in military and satellite applications. Another trade-off involves supply voltage. In general, a higher power-supply voltage means a lower on-resistance. For example, STMicroelectronics used a new process when fabricating the STG3699B quad-SPDT switch, giving it an on-resistance of 0.5Ω.

Another trade-off is power-supply current. A device that operates at high speeds requires a higher supply current to slew the transistor gates at a faster rate. CMOS or DMOS analog switches often have low power-supply current. For example, STMicro's STG3684 SPDT switch uses only 200 nA. This current rises with temperature. The company specifies some parts, such as the STG3689, at 85°C.

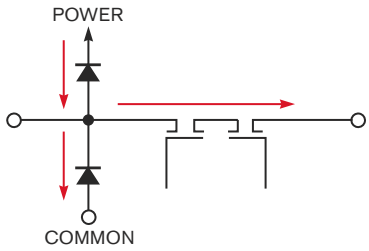

Figure 4 Leakage currents into a pin usually establish the off-resistance of an analog switch. This leakage comprises the leakage through the switch FETs and mismatch in the ESD-protection diode's leakages.

Other trade-offs include the size and power dissipation of the package. Switching-power designs require a larger package, which in turn may require a low on-resistance, because the bigger the die, the lower the resistance. Novel processes and circuit techniques have provided for remarkable strides in this area, as well. Vishay now offers 14 switches with on-resistances of less than 1Ω. Yet, these parts come in packages as small as SC-70 with a 3×2-mm footprint.

One trade-off that you may overlook is the change in on-resistance with the applied signal. If you use a high-voltage power supply and a small signal swing, then this change may not be a problem. If your signal swings rail to rail to the supply voltage, however, you will need a newer device that provides uniform on-resistance over the passed signal voltage.

CMOS analog switches tend to be cheaper but run on lower voltages. DMOS switches have higher voltages and switch faster. The DMOS switches generally have more stringent drive requirements. Vishay has developed the DG611 switch, which uses both CMOS and DMOS to achieve the benefits of both processes (**Reference 6**). One thing that distinguishes analog-switch makers is the ability to provide for custom or proprietary processes such as Analog Devices' 35V iCMOS process, which tailors the part for specific applications, according to Liam Ó Súilleabháin, a product manager at the company. "If you compare the ADG408 to our new product, the ADG1408, the 408 has an on-resistance of 100Ω, whereas the 1408 has an on-resistance of 4.7Ω. [The company offers] the 1408 in the same TSSOP package but also has another package option, the LFCSP, which is 70% smaller."

MEMS parts may involve a future trade-off for analog switches. The problems now are mechanical reliability and price. MEMS switches are mechanical, and, although you can expect them to be more reliable than a reed-relay switch, they can still wear out or fail catastrophically. Also, you must keep the MEMS structure away from the encapsulating epoxy, so MEMS packaging is always more expensive than silicon-analog-switch packaging. In addition, MEMS switches take longer to switch because they are mechanical.

Looking at the myriad applications and multifaceted specifications of analog switches, you can see that there is more than meets the eye with these ubiquitous little parts (**Reference 7**). Be sure to understand their uses and specifications when you design your next signal chain. If you are doing a Spice simulation that includes an analog switch, be sure that the model is complete, showing parasitic and stray capacitances and bondwire inductance. Many Spice models cannot account for charge injection or on-resistance change with applied voltage. Don't be surprised if the breadboard shows problems that the Spice run does not. Check everything over temperature and make sure that the part you have selected is available and will be in production for the life of your product. If you properly apply analog switches, you can achieve features and cost reductions that you cannot get in any other way. EDN

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RF: Will it ever be plug-in IP?

AS SOCs FOR MOBILE DEVICES INTEGRATE RADIO CIRCUITS, THEY WILL NEED TO REUSE RF IP. BUT WILL THEY BE ABLE TO?

BY RON WILSON • EXECUTIVE EDITOR

For the next generation of smart phones, mobile video players, and roaming Web accessories, integration means not just placing multipurpose basebands onto the same SOC (system on chip) with the application processor, accelerators, and memory, but also integrating the small-signal RF circuits of many radios onto the SOC. And therein lies a challenge.

In today's SOCs, reusing silicon IP (intellectual property) is absolutely necessary to meet schedules and maintain reasonable design complexity. But, although IP reuse is well-understood in the digital world and has even become common for some very-high-frequency blocks, such as SERDES (serializer-deserializer)

functions for high-speed I/O and PLLs (phase-locked loops) in all sorts of applications, design reuse is virtually unknown for RF circuits in radio applications. Why? And can you do anything about it? Or will the next generation of SOCs for mobile devices have to be largely custom chips?

SIZING THE QUESTION

At stake in these questions is a large fraction of the die area in the mobile-system SOC. This situation occurs not simply because radios tend to be large—with larger-than-minimum transistors and virtually unshrinkable inductors and capacitors—but also because the advanced handset will require lots of radios on one SOC.

For example, consider a typical concept device that acts as a multiband phone and Internet terminal, reaching out to whatever best connection is available at the time. Such a handset would have an LTE (long-term-evolution) radio for connecting to the cellular-phone network; an 802.11n MIMO (multiple-input/multiple-output) Wi-Fi-radio bank for making multiple-antenna connections to any available Wi-Fi access point; at least one UWB (ultrawideband) radio to implement Bluetooth, wireless-USB, or proprietary short-range, high-bandwidth protocols; and a GPS (global-positioning-system) receiver for obtaining location information. None of these components is trivial, and, in the case of the 802.11n MIMO radio, the area is substantial (**Figure 1**).

Initially, these radios may all be on separate dice. But design pressures will force many, if not all, of them to migrate onto the SOC. The exception will be the large-signal RF blocks, such as power amplifiers and antenna switches, which are likely to remain off the SOC.

The small-signal RF blocks in a typical radio are not hard to enumerate (**Figure 2**). They recur in about the same configuration in most modern radios. But that situation does not mean that it's easy to reuse either a whole radio block or the individual functions.

With so much complexity, so much die area, and so much at stake, it would seem obvious that SOC designers—particularly SOC teams that lack internal RF expertise—would want to obtain their radio blocks as third-party IP. But the reality is that, today, they will not. And even in the moderate-term future, some or most of the radio blocks in these SOC designs will be the work of the SOC-design team itself, not a third-party-IP developer. There are several important reasons for this predicament.

All of these reasons follow from the concept of reusable IP. To be reusable, an IP block must have a clearly understood function, upon which the creator and the user agree. It must have clearly defined ports, and the signals at these ports must be unambiguously defined both as to their relationship to the function of the block and as to their allowable signal characteristics. Without these basic constraints, IP is not so much reusable as redesignable. But, as you will see, each of these requirements is problematic for RF-radio IP.

The first problem is the matter of standards. Certainly, there are clear air-interface standards, with verification IP and interoperability tests, for virtually all nonproprietary air interfaces. But the problem is the implementation of the radios. "The transceiver architecture for these standard radios is still evolving," warns Berkeley Design Automation Chief Executive Officer Ravi Subramanian. "How you want to build the radio still depends on the market you are going to serve with it." For example, a UWB radio, although structurally much like an 802.11 radio, can look different in detail (**Figure 3**).

AT A GLANCE

- The next generation of mobile wireless devices will depend on integration of some radio functions into the SOC (system on chip).
- SOC development depends on IP (intellectual-property) reusability.
- RF circuitry is notoriously hard to reuse for some very compelling reasons.
- Reuse of third-party-radio blocks is likely to be difficult and slow to emerge.

"Even standard radios are less well-defined than you might think," says Navraj Nandra, mixed-signal-product-marketing director at Synopsys. For instance, he notes, different countries might implement the same standard radio differently. WiMedia radios in the United States use Band Group 1. Other countries use higher-frequency band groups requiring different radio designs.

"And, putting these radios into CMOS on an SOC is the crown jewel for the companies that can do it," Subramanian says. "The ability to integrate the radios with high performance is essential to their products, and it differentiates them. They are not going to buy the radios as IP, even if they could."

But what about licensing the subblocks within the radios? After all, you can license third-party PLLs that run as fast as some of these blocks. That scenario is not in the cards either, Nandra says. "There are clear functional blocks in a radio: the RF front end, the mixers, the data converters, and so on. But the problem here is that the exact partitioning into blocks, and the interfaces between them, is not defined. For example, in the PCI [peripheral-component-interconnect] Express world, there is an industry-standard pipe interface between the PHY [physical] and the MAC [media-access-control] layers. But the interfaces between the functions in radio hardware are not defined."

"These are very difficult interfaces," says Carlos Leme, executive vice president of the wireless-systems group at MIPS. "It's not a matter of just plugging them together. You have to observe all the loading and impedance-matching requirements of the RF signals between blocks."

The functions within the blocks also are not clearly defined. "The partitioning of RF circuits is very complex," Leme continues. "The specifications of the blocks interact with each other." Leme explains that, for example, skilled RF designers may choose to accept more noise in one portion of a circuit and make up for it in another. "[For this reason] there has never been a significant market for RF-building-block IP," Leme adds. "You always end up having to work closely with the design team; it's not really IP then."

SIGNALS AND NOISE

Even if a design team would accept previously defined building blocks, the integration process would prove difficult. The problem involves another component of the definition of reusable IP: The block should have well-defined signals on clearly defined pins. The difficulty with this concept for RF design is that interactions between an RF circuit and the rest of the chip don't involve only defined signals or even intentional paths between the IP block and the rest of the chip. This situation can lead to interesting problems.

First, there is the connection problem. You can't simply tell a digital-routing tool to connect the pins on a hard-IP block to their destinations and end up with a working radio. RF-signal paths must have impedance matching. They care about parasitics. And they care—

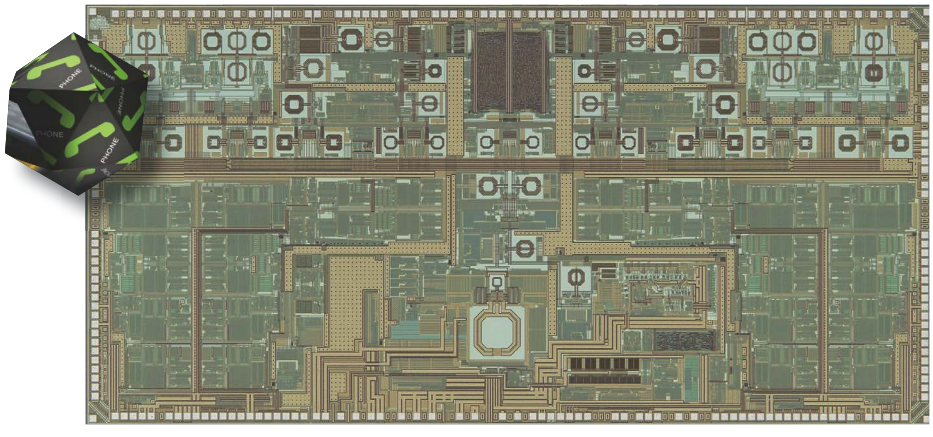

Figure 1 The Broadcom BCM2055 is a 4×4 MIMO radio supporting the 802.11n draft specification. Note that both complexity and die area are not insignificant.

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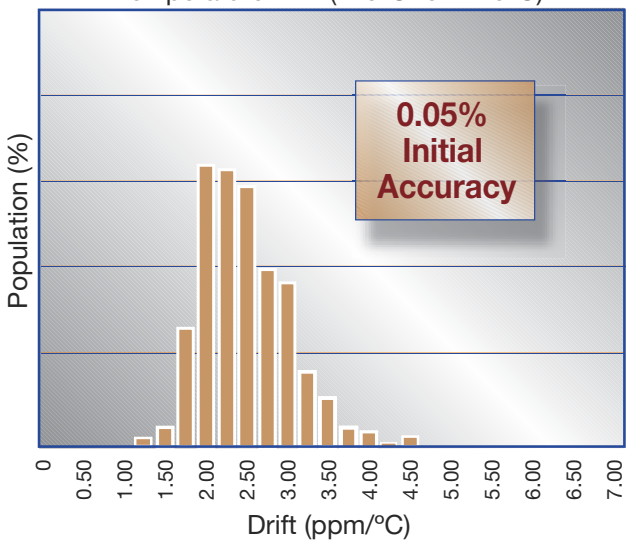

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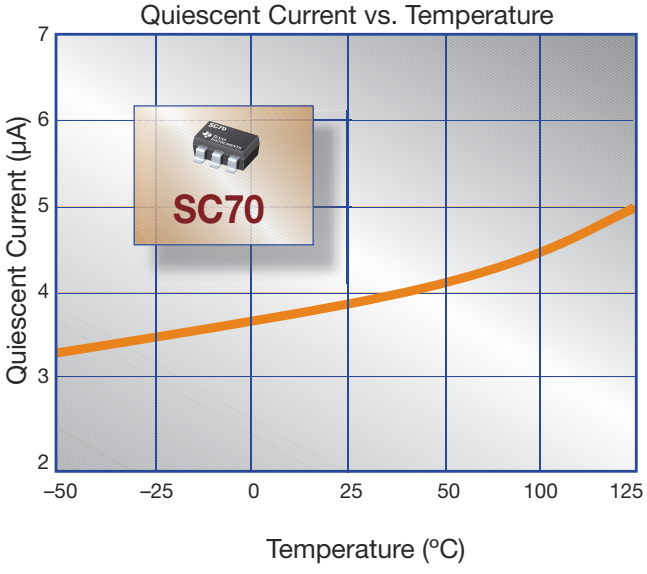

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REF32xx	0.2	1.25, 2.048, 2.5, 3.0, 3.3, 4.096	7	100	±10	SOT23-6	$1.70
REF31xx	0.15	1.25, 2.048, 2.5, 3.0, 3.3, 4.096	15	100	±10	SOT23-3	$1.10
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sometimes a great deal—about everything that is going on at the node to which you attach them.

Even with impedance-matching connections to quiet, well-behaved nodes, a piece of hard IP validated in the process you are using may not behave in your chip as it behaved in the test chip. Often, this unpredictability is due to interactions between the RF circuitry and the rest of the die that don't involve the defined signal paths.

"Models are problematic in RF design," says Hany El Hak, senior product-marketing manager at Cadence. "It's not because the RF models you get from the foundry or the IP vendor are inaccurate, necessarily. It's because the assumptions the IP designers made while constructing the models don't always get communicated to the IP user."

He explains that, for instance, if the IP designer assumed a maximum supply-noise figure, you need to know it to verify that the supply pins on the IP in your design don't exceed that figure. "In general," he notes, "the problem is that, in the RF domain, there are couplings and interactions that don't follow the signal path."

Supply noise is just one example El Hak offers. Another is substrate coupling. Until recently, it was all but impossible to get accurate substrate models for even the best CMOS-logic processes. Now, those models exist, and foundries are happy to share them, El Hak reports. "But substrate-coupling models are very complex. If you include them in your circuit models, the complexity of the overall problem explodes. You must have some formal way of reducing the complexity of the model—removing parasitic paths to which the circuit isn't particularly sensitive—to make simulation feasible. There are tools to [accomplish this task], in Spectre, for example. But it's not fully automatic. The accuracy of the reduced model still depends on the designer's guidance in pruning the circuit."

VERIFICATION ISSUES

With all the potential for interactions between a radio-IP block and the substrate, the supply pins, the signal pins, and even nearby but unrelated traces, it should be no surprise that even experienced RF designers approach verification of the integrated block with a certain amount of respect. There is no easy way out.

"You really want to do verification of the whole system, not just the IP block," warns Irshad Rasheed, president and chief executive officer of RF-design-services house Tahoe RF Semiconductor. "Just defining the system from the top level can be 15 to 25% of the design cycle. Once you [define it], many design teams begin to analyze the system from a behavioral level with Verilog models and with enough extracted data to allow an analog/mixed-signal functional simulation." Moving directly to integration of the IP and producing GDS (graphic-data system)-II for the whole chip is possible but extremely risky, he cautions. "Models for substrate coupling and for the noise spurs from the digital circuitry are never that good. The VCOs [voltage-controlled oscillators] are never centered. The risks are very high."

Instead, Rasheed recommends, the design team can implement the radio circuitry on test chips. These components can start out with small structures simply to validate the circuit models and progress to an entire radio block surrounded by digital-noise generators

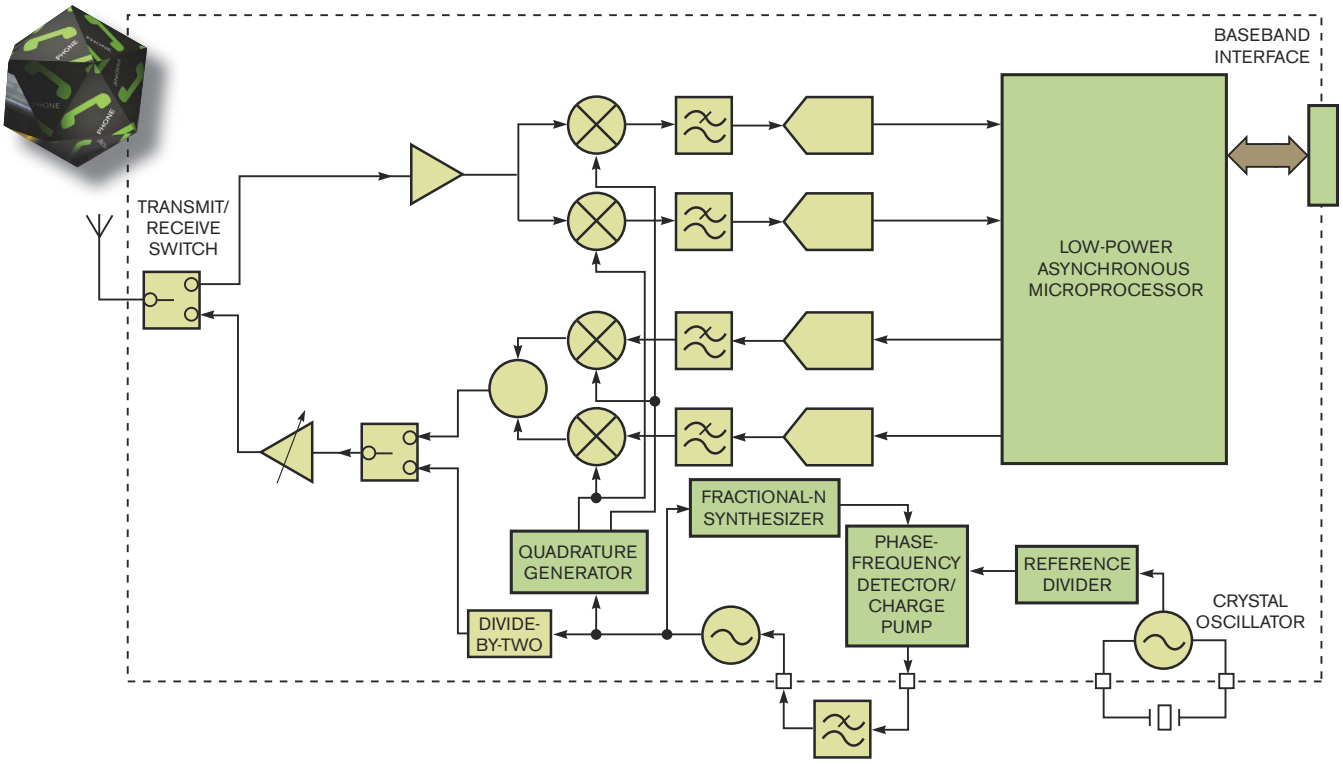

Figure 2 A typical two-way radio block shows the major functional subblocks (courtesy Berkeley Design Automation).

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to simulate the environment on the final SOC. "With test chips, you can verify a great deal of the radio behavior before you find yourself signing off on final masks for an entire SOC," he says.

In any case, Rasheed emphasizes the importance of top-level simulation that is both abstract enough to view the behavior of the design as a working radio and accurate enough to predict problems. "You need Verilog-A models that reflect circuit-level reality," he says. "[Achieving that goal] takes a lot of experience in RF synthesis. It takes moving back and forth easily between Spectre, RF-Spice, and Verilog-A models. And it takes knowing where the 'gotchas' will be so you can capture them in the higher-level models and not be surprised by them down the road. Realistically, the RF designers must be involved in the chip-verification process."

Reflecting the difficulty of the verification task, Berkeley Design Automation's Subramanian describes five phases of verification for RF IP: functional simulation, performance analysis, noise analysis, investigation of the interactions with package design, and analysis of sensitivities to process variations. Unfortunately, although you need to complete the first two of these steps on the block preintegration, all five are necessary after integration and layout of the SOC.

VARIABILITY

And then there is the matter of variability—not just process, voltage, and temperature variations, but also package and board variations. A radio you drop into an SOC must work in the digital-CMOS process in which you fabricated the SOC. But it must function within all the process corners for that process. And it must work in all the package variations marketing may dream up for the chip. And it must work in the customer's board design.

RF designers have two fundamental weapons in this unequal battle: robust circuit design and digital configuration. The first of these factors, circuit robustness, has been a tool of RF designers since the days of vacuum tubes. It is a matter of solid circuit-design experience, adequate simulation, and, many designers argue, enough test chips. But with the integration of RF circuitry into digital-CMOS processes, designers have a new weapon that has changed the nature of radio design: digital configurability.

"Radios are very sensitive to parasitics, and parasitics are neither stable across process variations nor accurately modeled," argues Leme from MIPS. "We need improved design kits with more parasitic data. But even so, in the end, you will … [be] using digital trimming to center the circuit to the process. We try to add as much configurability as possible to the IP."

Leme says that advanced CMOS processes help with adding configurability. "Once you get to 90 or 65 nm, analog switches are very good. You can use them without badly degrading signals." This ability has opened the door to a design style in which digital signals can open and close switches not only to adjust bias currents or match impedances, but also to switch active elements into or out of the signal path.

This style is new to RF design, accord-

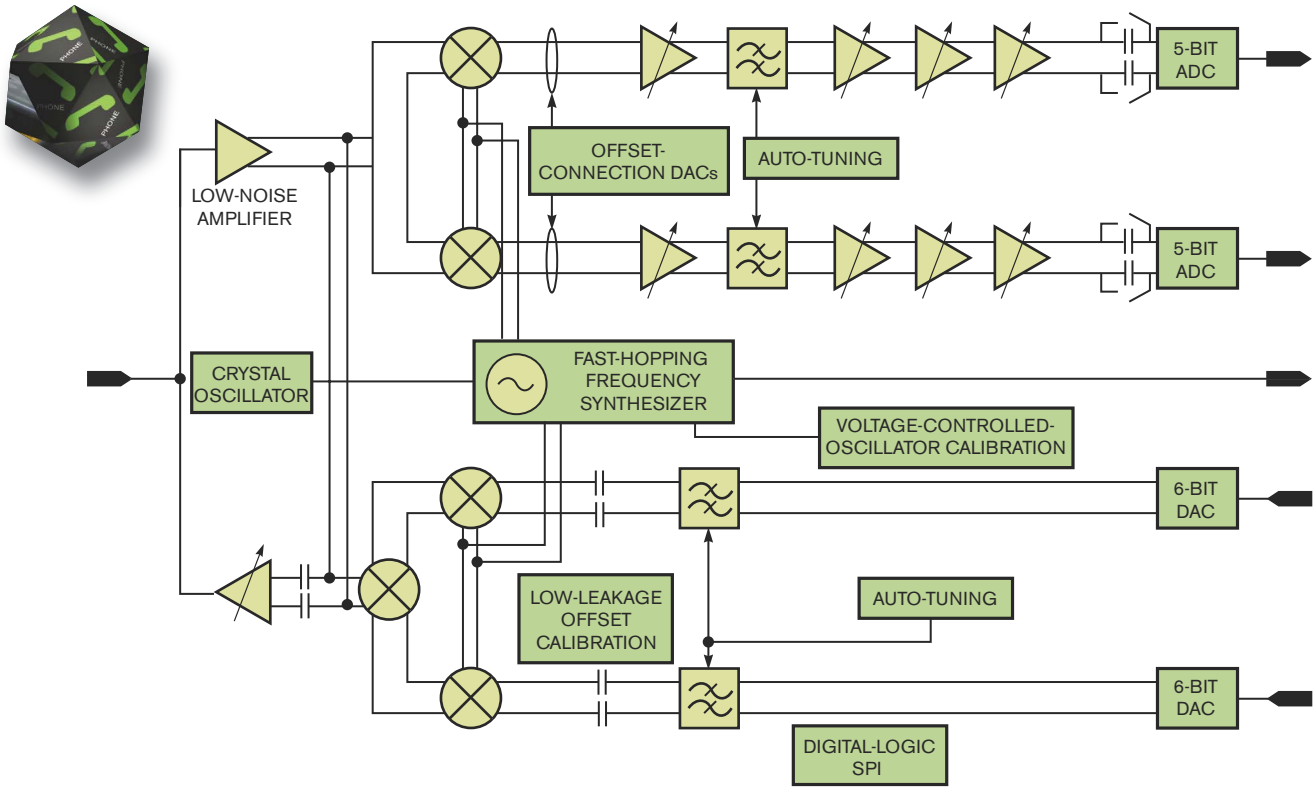

Figure 3 A UWB transceiver follows the basic pattern of the design in Figure 2 but adds functional blocks to support the UWB air interface (courtesy MIPS).

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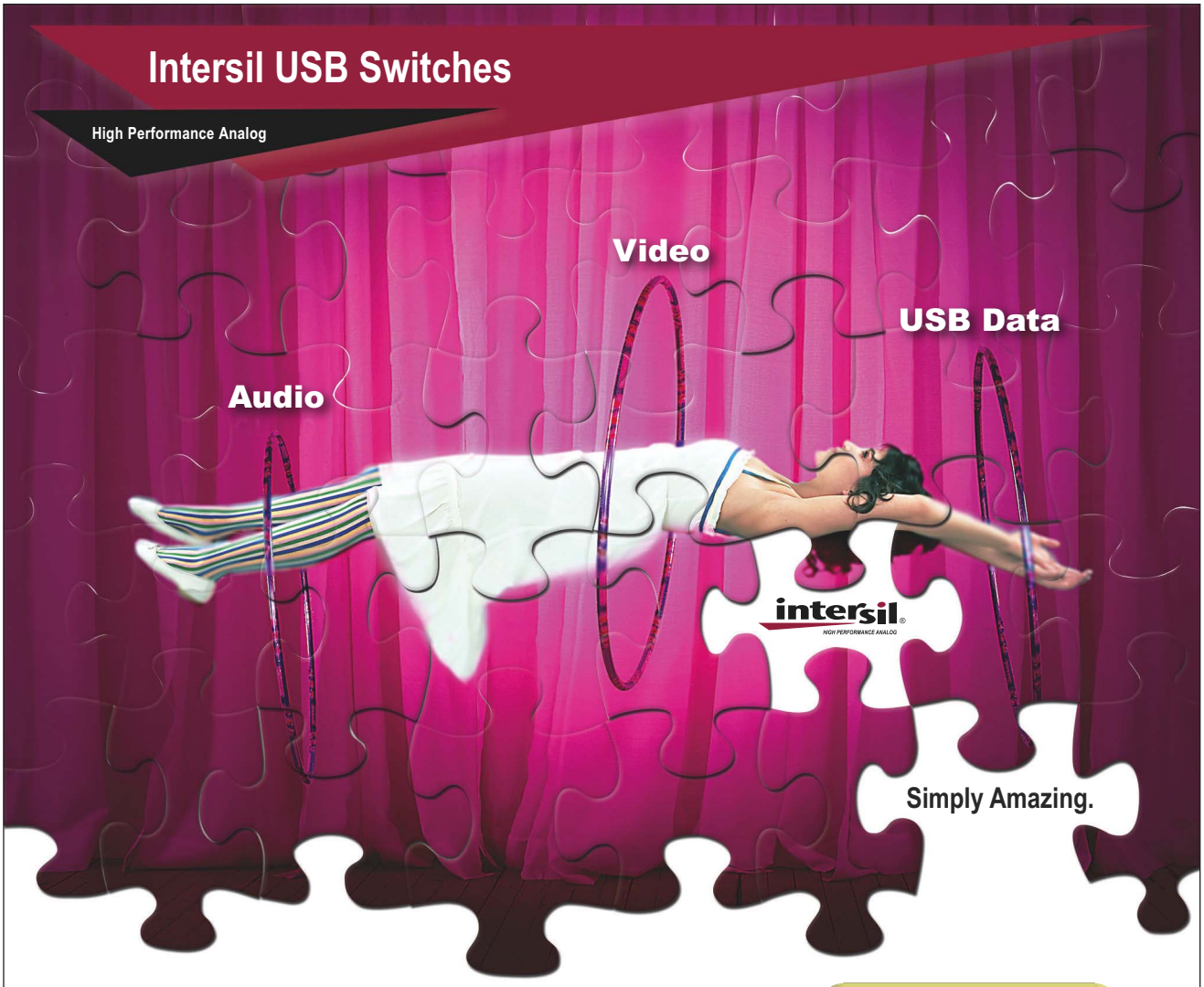

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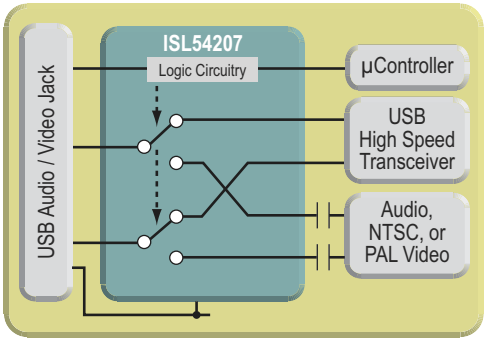

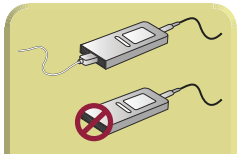

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ISL54208	0.06	480	0.28 / 0.04
ISL54415	0.007	12	0.04 / 0.03
ISL54416	0.007	12	0.04 / 0.03
ISL54417	0.007	12	0.04 / 0.03

Audio / Data

Device	Audio THD 32Ω (%)	USB Speed
ISL54205A	0.06	480
ISL54206	0.06	480
ISL54400	0.007	12
ISL54401	0.007	12
ISL54402	0.007	12

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ing to Subramanian. "Advanced CMOS processes have their limitations for RF, but they give you a huge number of transistors to play with," he says. "That [abundance] has led designers into the practice of throwing transistors at any inability to reach specifications. Consequently, RF-CMOS circuits on an SOC tend to be much larger than traditional RF designs: You can see 100,000 transistors in one of these things."

In this new design style, configurability takes up the slack for imprecise knowledge of critical parameters at design time. For noise, in particular, Synopsys' Nandra says, models are a problem. "Gate noise is the primary issue. If you are starting a design early in the process life—as aggressive SOC designers tend to—the transistor-level noise models may not be exactly stable. It's a good idea to drop some process-monitoring devices into the scribe lines on test chips to help calibrate your models. Then, you can include the test structures in your IP further down the road to aid in calibration." And the data from those structures can set digital parameters that center the circuit.

TOWARD IP REUSE

That application of massive numbers of transistors, performance monitors, and calibration circuits into RF design has changed the nature of radios from elegantly small circuits with only a few active devices to incredibly complex digital circuits with only a few RF devices on the signal path. This evolution has moved us toward the goal of reusable RF IP.

Arya Behzad, distinguished engineer and director of engineering at Broadcom, bluntly sums up the current situation: "It would be impossible to produce our product lines if we could not reuse IP. But, typically, RF IP requires more changes during reuse than digital or other analog IP." Behzad says that this reality has led Broadcom RF-design teams to consciously design their radio blocks for reuse—depending on the application. "If we are designing a radio for a completely new market area, and we just want to get some experience, we may do a one-off design," Behzad says. "But, if we are developing a full product line for a market in which we have some experience, we will aim for reuse, even though this costs some die area. The concept is to take advantage of all those short-channel devices, and use lots of them to make the radio flexible. You end up with a ton of circuitry around the core."

IT SHOULD BE POSSIBLE TO MAKE A RADIO CONFIGURABLE ENOUGH TO REUSE ACROSS A VARIETY OF SOC DESIGNS.

Area and power are obvious costs of this flexibility. So design for reuse is not a dogma but yet another engineering trade-off. "For instance," Behzad offers, "if you do the blocks for a radio with reuse in mind, you may find that 70% of the blocks you designed for a single-in, single-out radio you can reuse in a MIMO radio, even though the requirements for the MIMO radio are more severe."

Assuming that you have designed the radio for reuse, integration becomes a process of matching up the configurability of the IP to the requirements of the new SOC, Behzad explains. But this process in itself can be complex. He points out one 802.11n transceiver that has more than 2 kbits of digital control. "And many of those bits interact with other parts of the chip in real time," he explains. "To verify operation in a new environment, you have to move between Verilog-A models; digital simulations; and, in some interactions, transistor-level simulations. We've found that this [requirement] becomes particularly an issue with initialization sequences."

Behzad says that validating coupling between blocks is another hard part. "It's impossible to capture everything—for instance, substrate or package coupling. The problem is that you really need to model the die, package, and circuit board together. It becomes a monster model, and the simulations won't run. So you make some simplifying assumptions, [which] open the door for mistakes.

"You can't get the simulations right to the last decibel," Behzad warns. "So, you work at the beginning to make the circuit less sensitive to the things—[such as] noise spurs—that are difficult to predict or just impossible to stop." For example, Behzad says, there is substrate coupling. "There are more claims than realities on the tools for modeling substrates," he laments. "So, you use your experience [to determine] when to add substrate capacitors, put in guard rings, and use N wells. Where you can't predict, make the design robust."

Will all of these steps make an RF-IP block reusable? "Within a company, definitely, yes," Behzad says. "But with third-party IP, I think not."

The question at last comes back to Subramanian's point about differentiating versus commodity radios. It seems likely that, with the relatively standard operating voltages, extremely high cutoff frequencies, and enormous transistor counts of 65- and 45-nm processes, it should be possible to make a radio configurable enough to reuse across a variety of SOC designs. It might even be feasible to make the IP relatively portable across foundry processes, although some designers are pessimistic that this approach will ever be practical.

But Subramanian emphasizes that it will never be possible to make a radio at once configurable enough for reuse, small enough and low enough in power for a critical application, and offering high enough performance for the radio to help differentiate the finished SOC. "Over time, I think we will see Bluetooth, GPS, and maybe television-tuner blocks become commoditized enough to be third-party IP," Subramanian speculates. "But for applications where the radio's performance helps differentiate the end product, I think third-party IP will always be unlikely."EDN

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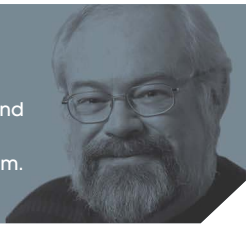

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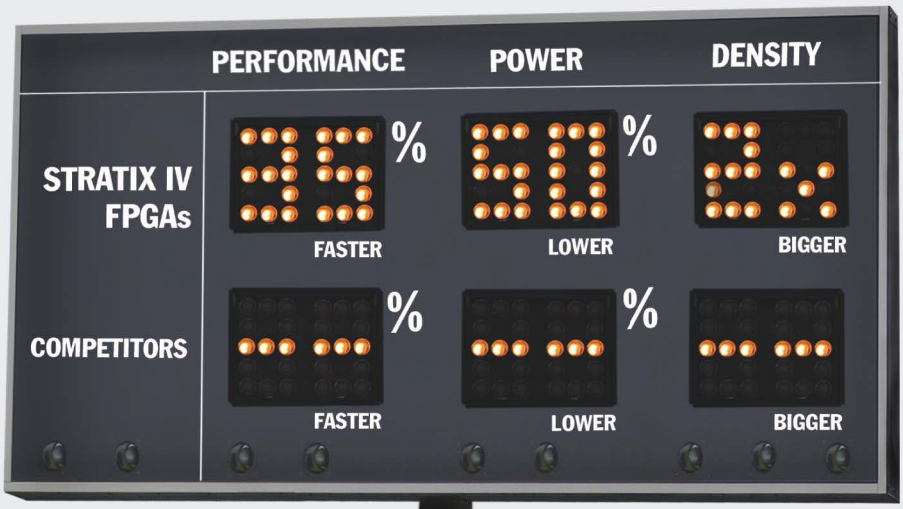

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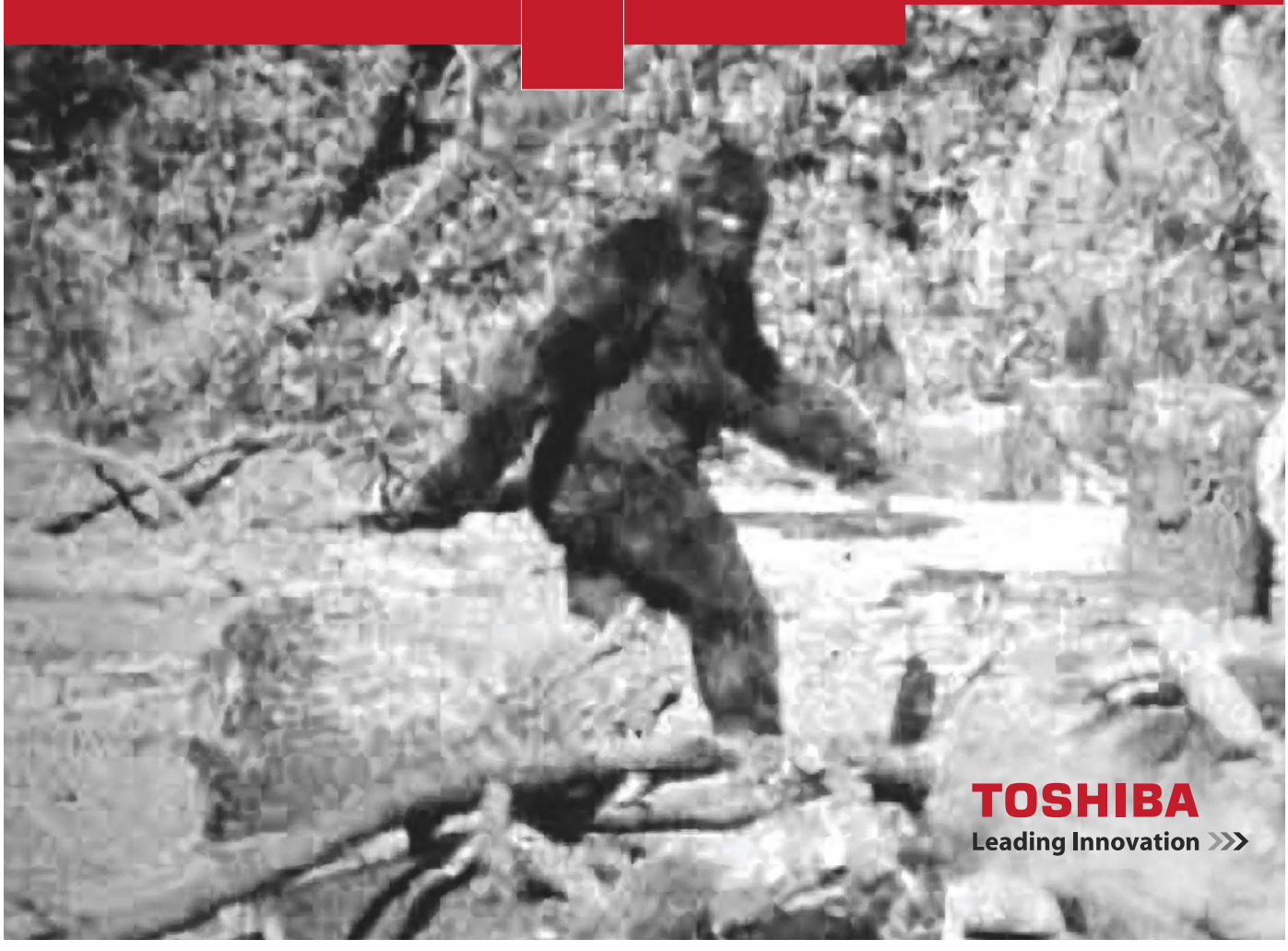

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BY MOJY CHIAN, RICHARD CLIFF, AND JEFF WATT • ALTERA CORP

Achieving first-time success at 40 nm

AN EARLY ADOPTER AT THE 40-NM NODE TELLS WHAT IT TOOK TO GET RESULTS FROM THIS LEADING-EDGE PROCESS.

Every process generation brings new design challenges, but, for the 40-nm node, both the difficulty and the risks are exceptional. Increased complexity, size, and design costs dictate that designers adopt new methodologies to ensure that they get it right the first time (**Figure 1**). Systematic use of test chips and enhanced statistical simulation are some keys to successfully addressing 40-nm-process-generation challenges.

Designers moving to adopt a 40-nm-process technology face substantial risks. The new process comes with new design challenges to address, and the penalty for error is high. Mask costs grow about 50% each generation, and, for the 40-nm process, they currently exceed $3 million. Equally important, the cost of the design effort is growing—more rapidly than mask cost—because of increasing gate count and chip complexity. Designers, therefore, need to adopt methods that will allow them to address both the financial and the technical challenges of process migration (see **sidebar** "Bimodal-process-technology adoption").

One of the most important moves that design teams can make is to adopt a methodology of verifying blocks in silicon using test chips early and often during the design. Altera (www.altera.com) adopted this approach for the 90-nm generation and has carried it over to the 65- and 40-nm generations to achieve high success with first production silicon. The approach supports design reuse to save development cost and helps the design team understand and resolve new process-design challenges (see **sidebar** "Analog challenges versus process-node shrinkage" in the Web version of this article at www.edn.com/ms4291).

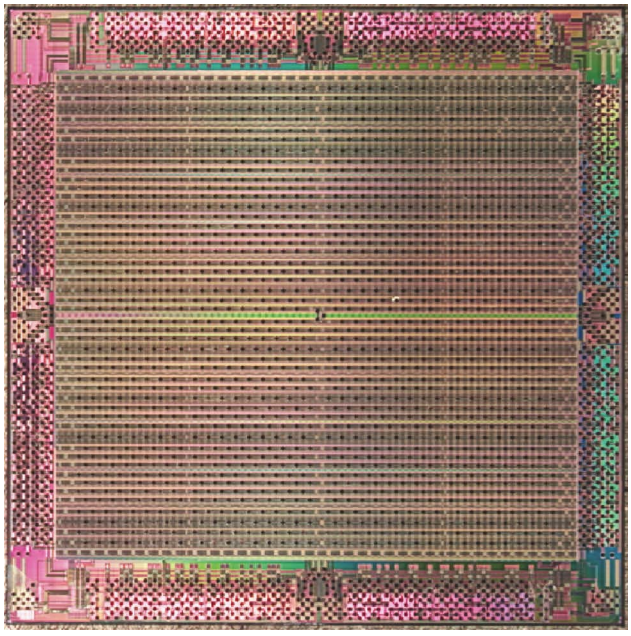

Figure 1 A 40-nm FPGA results in increased complexity, size, and design costs that require designers to adopt new methodologies.

TEST CHIPS SOLVE PROBLEMS EARLY

Test chips help address numerous design issues by validating both the circuit design and the process characteristics (**Table 1**). The first test chips, which designers run early in their efforts, can contain simple logic blocks and interconnects or single transistors. The design of these test chips can begin before the process and simulation models are stable, giving developers a head start on process migration. These tests help validate some design rules and indicate where other rules need modification, ensuring that the circuitry will perform as expected in the final design. Testing at this stage, however, requires design teams to work closely with their foundry to understand the deep-submicron issues that arise.

TABLE 1 TEST CHIPS AND THEIR FUNCTIONS DURING THE 40-NM RESEARCH AND DEVELOPMENT EFFORT

Test chips	Tapeout	Major components
TC1	Fourth quarter, 2005	Early technology assessment, OPC
TC2	Third quarter, 2006	Transistors and modeling
TC3	Fourth quarter, 2006	FPGA fabric, transistors, modeling
TC4-a	Third quarter, 2007	I/O, analog, FPGA fabric
TC4-b	Third quarter, 2007	Complete FPGA
TC5	Third quarter, 2007	Transmitting and receiving analog sections of the transceiver
TC6	Fourth quarter, 2007	Memory
TC7	Fourth quarter, 2007	On-chip regulators
TC8	First quarter, 2008	I/O, lab, FPGA fabric

Test chips also help to account for new deep-submicron effects that arise with a change in technology node. Sometimes, these new effects become more apparent in actual circuits than they were in simple process-test structures. Then, a test chip behaves unexpectedly. By undertaking a correlation exercise, the design team can help identify effects they had not previously understood. Test chips can also identify circuit sensitivity to effects that the designers knew about but did not fully appreciate.

Later in the design process, when all important effects are known and when the design rules are more stable, test chips allow designers to evaluate larger blocks. At this stage, teams can also try to reduce design layouts or new layouts of logic designs to determine whether they function adequately in the new process. The results of such tests help teams define their strategy for both hard- and soft-design reuse to save development time and cost. If functional problems appear or the block's performance needs improvement, designers have an opportunity to make the necessary changes early in the project. Blocks that traditionally need fine-tuning include memories, PLLs (phase-locked loops), and high-speed I/Os. They are prime candidates for testing at this stage.

As the design progresses, test chips allow designers to evaluate the integration of blocks into larger structures. The chips also provide an opportunity to evaluate any modifications the team made as a result of earlier testing. Depending on how many test chips they run during the development effort, designers may have several opportunities to repair or enhance their blocks before the design becomes final. Altera's development efforts may involve as many as nine test chips during a product design, typically every three to four months.

This use of test chips greatly increases the chances for first-time success when you fabricate the full design, but the approach might appear costly at first because it involves so many mask sets. Collaboration with the foundry as well as the use of shared-cost programs, such as the TSMC (Taiwan Semicon-

BIMODAL-PROCESS-TECHNOLOGY ADOPTION

The data in Table A shows the percentage of ASIC-design starts each year by process-technology node. Gartner (www.gartner.com) gathered the statistics for 2007 and made projections for the future. Each column totals 100. The most popular design-process node has for some time been 0.13 microns–based on the fact that 0.13-micron designs offer enough integration density, performance, and reasonable NRE (nonrecurring-engineering) costs for most designs. Designs at 90 nm and beyond are more expensive and riskier, and they require careful power management. It is not easy to balance ROI (return on investment) for many ASIC designs. The right axis in the table includes Altera's estimates for the total NRE cost for an ASIC at each node. These costs include masks; design; test; and software development, including labor, software, and hardware costs. As these costs increase, so do risk and development time.

Contrast this situation with FPGA development. A few years ago, when older technology was in use, FPGAs stayed behind the ASIC-technology curve. Today, FPGAs are ahead of the curve. In the future, there will be a three-process node or more process-technology advantage–invaluable for customers who may compare ASIC and FPGA technology for a given design. Examining cost, density, and performance, you can make no comparison between a 0.13-micron ASIC and 45- or 32-nm technology.

With only a small investment in software-development tools, customers can gain access to the latest process technology. These products are programmable and available to tens of thousands of customers, whereas an ASIC is available to only one customer. FPGAs maintain a better ROI, thus allowing the manufacturer to steadily invest in newer technologies. The ultimate result is that more designs will migrate from ASIC to FPGA technology, taking advantage of time to market, cost, performance, and power and significantly reducing risk and NRE costs.

TABLE A ASIC-DESIGN STARTS BY PROCESS-TECHNOLOGY NODE

Process node (microns)	2002 (%)	2003 (%)	2004 (%)	2005 (%)	2006 (%)	2007 (%)	2008 (%)	2009 (%)	2010 (%)	2011 (%)	Development costs ($M)
0.022	0	0	0	0	0	0	0	0	0	0	110
0.032	0	0	0	0	0	0	0	1	2	2	80
0.045	0	0	0	0	0	1	2	4	6	7	60
0.065	0	0	0	1	2	6	8	10	13	15	55
0.09	0	1	8	13	18	23	23	24	24	24	30
0.13	18	37	42	29	29	27	27	25	24	24	20
0.18	38	27	23	20	17	14	12	10	10	8	13
0.25	16	15	12	12	11	9	9	8	7	6	5
0.35	21	16	12	12	11	10	8	8	6	5	3
0.5	5	4	3	7	7	6	6	5	4	4	2
More than 0.5	1	1	0	6	6	6	5	5	5	5	Less than 1

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ductor Manufacturing Co, www.tsmc.com) Shuttle program, however, can keep down the cost of test chips. During process development, for instance, the foundry must run numerous test wafers to fully characterize and tune its fabrication methods. It also periodically runs test wafers to monitor the process. A close working relationship with the foundry provides opportunities to piggyback simple test structures on the foundry's own wafers in the early stages of a design. The Shuttle and similar programs allow testing of larger structures or even full designs. A 3×4-mm die in a 40-nm shuttle costs less than 5% of a full mask set, allowing several iterations of the final design for less than the price of one production-mask-set revision. The total mask cost of the test-chip program may exceed the cost of one mask-set revision, but the design-effort efficiencies you gain in areas such as design reuse and early error detection can largely offset the test costs.

Along with adopting new design methodologies such as the test-chip program, developers embracing 40-nm technology need to enhance their methods and design parameters. Three areas that are particularly important in this process generation are process variability, power management, and high-performance analog. Although these problems are well-known in earlier process generations, 40-nm technology puts a unique spin on them.

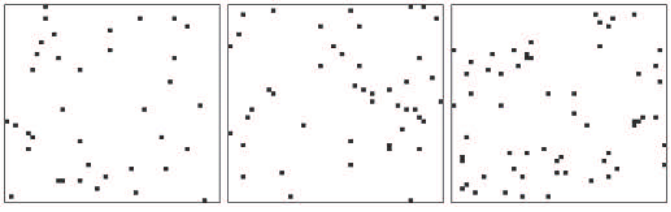

Figure 2 Trial plot diagrams show a random distribution of doping atoms in a 40-nm-transistor channel.

LOCAL VARIABILITY BECOMES SIGNIFICANT

Chip developers have long been aware of and have accommodated process variability at the chip level. Monte Carlo statistical simulations guide designers in creating chips that will work properly when their transistors vary as much as three standard deviations (three sigma) from the production mean. But these techniques address only wafer-to-wafer variations and chip-to-chip variations within a wafer. In a 40-nm process, features are so small that the placement of individual atoms can have a measurable impact. Gate oxides, for instance, are now only a few atoms thick. You can no longer consider the dopant in transistor channels relatively uniform. Instead, the placement more closely resembles a dash of salt grains scattered across a plate, on which each outlined square is one random distribution with an expected value of 50 dopant atoms (**Figure 2**). The actual number of atoms—37, 45, and 60, respectively—for these three trials shows that, in addition to having a random spatial distribution, the total number of atoms within each square varies.

This dependency on individual atomic placement introduces an unprecedented degree of local variability to circuit

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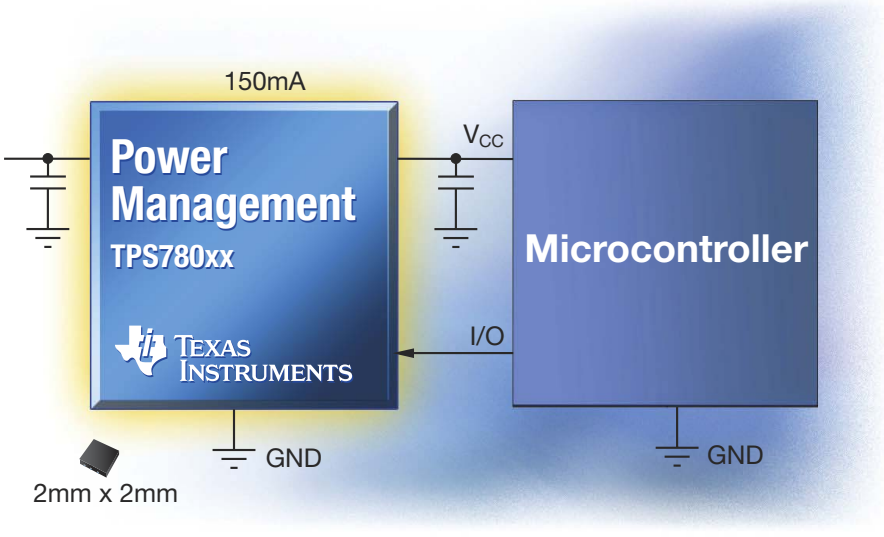

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TPS797xx	1.8 - 5.5	10	1.25 - 4.9	1.2	SC70	$0.34
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behaviors. Robust statistical-analysis and modeling tools, which accurately account for local variation, enable designers to optimize their circuits in the presence of local variability. The ability to accurately model local variation is especially critical for the design of high-yielding memory and analog circuits. For parameters such as standby current, only the total current across a die is valuable. In this case, local variations above or below the average tend to cancel each other out.

In addition to designing for greater variability, developers should begin to incorporate redundancy to improve chip yields. This step is particularly important for the large dice of today's complex designs. With a large die, even a small change in the defect density in production can have a major impact on yield. On-chip redundancy allows the design to bypass defects instead of simply failing. You need to weave this redundancy into the architecture at the circuit level, however, not add it as an afterthought.

Developers should also consider lowering the circuit power. As process technology shrinks, circuits become faster and denser, and chip power rises in proportion. For many applications, however, chip power is more important than performance. Many applications require more functions in next-generation chips without increasing power requirements, and higher performance holds only secondary importance.

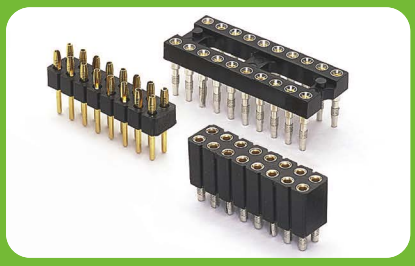
The traditional approach to lowering power has been to lower the supply voltage to offset the greater number of transistors. But transistor-threshold levels do not scale with process technology, so lowering the supply voltage reduces the margin within which the transistor operates. Local variations further reduce that margin. The lower the supply voltage, the greater the significance of predicting and accounting for local variability—specifically, for threshold-voltage variations.

TRADING PERFORMANCE FOR POWER

In addition to lowering supply voltage, designers must adopt other approaches to reducing chip power. Altera has traded performance for power at both the transistor and the architectural levels. Increasing the threshold voltage of a transistor, for instance, slows it but reduces its leakage current. Similarly, increasing channel length slows a transistor but lowers its switching current. You can make numerous other such trade-offs at the transistor level.

At the architectural level, designers can trade performance for power on each circuit. In an ASIC design, this kind of trade-off is static. Analyzing the performance needs of a circuit identifies the critical paths on which high speed is necessary, allowing designers to assign faster transistors on those paths and use slower but less power-hungry transistors elsewhere. In an FPGA for which you don't know the critical path before programming and in other applications in which circuit speed

MAXIMUM



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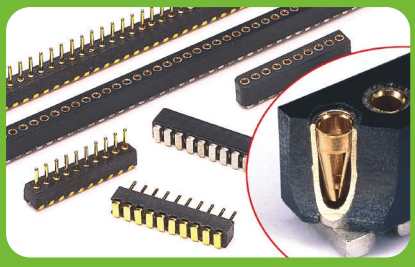

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may vary, a more dynamic trade-off is necessary. Reverse-back-biasing a transistor increases the threshold voltage, thereby reducing the power. Design tools can automatically adjust the back bias of the transistors based on a specific program to optimize speed and power.

THE MIXED-SIGNAL PROBLEM

Finally, designers must address the challenges of mixed-signal design. Many devices now need to incorporate high-speed transceivers. Even for purely digital logic, analog and high-frequency circuit content is increasing to support such functions as high-speed serial I/O. Successful implementation of such functions requires circuit components optimized for high-speed-analog-circuit design, but their requirements are often at odds with the requirements for high-speed-digital-circuit components. This discrepancy is becoming more pronounced as process technology scales down.

The key to solving this dilemma is working closely with the foundry early in process development to ensure adequate optimization of the essential components for high-speed-analog design. Developers can also populate a significant portion of their test chips with analog components to help develop accurate simulation models. Placing one whole channel of a high-speed transceiver on a test chip, for instance, gives an opportunity to evaluate the parasitic effects of interconnects; model on-chip resistors, capacitors, and inductors; and see how well the design will work. This use of test chips allows designers to predefine analog components and fully characterize them to minimize mismatches in the final design.

Collectively, all these efforts addressing analog design, power trade-offs, local variability, and the use of test chips work together to ensure first-time success in 40-nm design. Further, the methods that address these problems will be applicable when it comes time to make the next process migration. New technical challenges will arise, but the methodology provides the opportunities to resolve those challenges, keep costs down, and achieve success with first production silicon. EDN

AUTHORS' BIOGRAPHIES

Mojy Chian is vice president of technology development at Altera Corp. His responsibilities include process-technology definition, implementation, and design infrastructure for new technologies, as well as yield improvement, defect-density reduction, and factory control for mature technologies. He holds bachelor's, master's, and doctorate degrees in electrical engineering as well as a master's degree in applied math from the Florida Institute of Technology (Melbourne, FL).

Richard Cliff is vice president of IC design at Altera Corp. He has led the hardware development for the Stratix, Apex, and Flex device families and holds more than 100 patents in programmable logic. He has a bachelor's degree from Manchester University (Manchester, UK).

Jeff Watt is a technology architect at Altera Corp, where he oversees compact-model development. He has master's and doctorate degrees in electrical engineering from Stanford University (Palo Alto, CA) and a bachelor's degree in electrical engineering from Queen's University (Kingston, ON, Canada).

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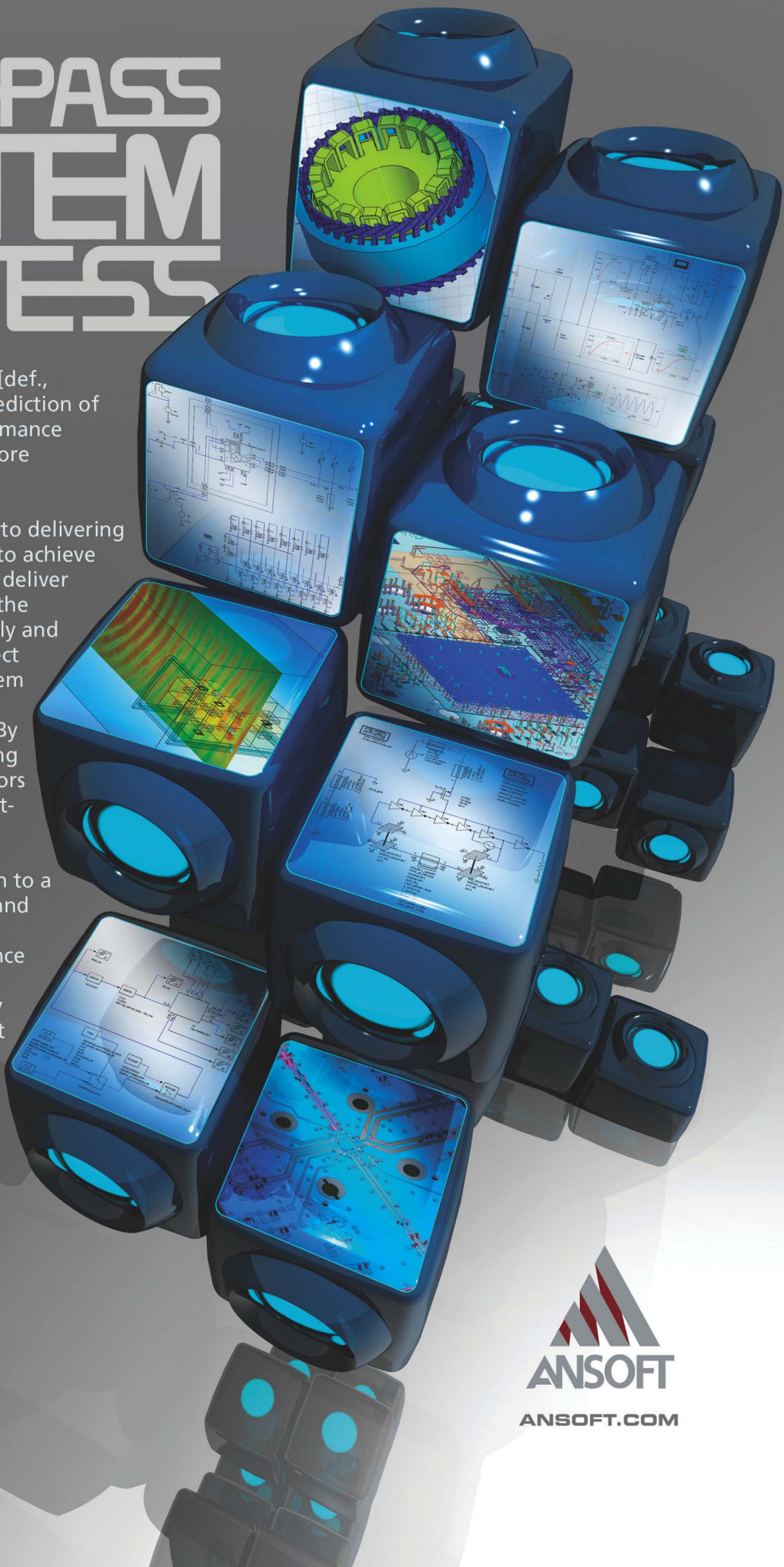

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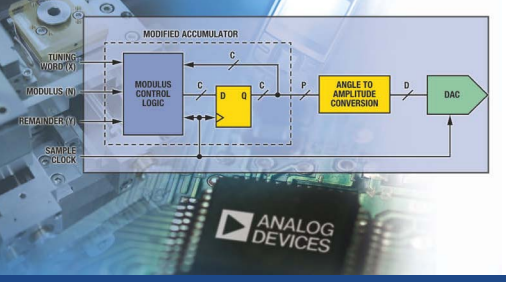

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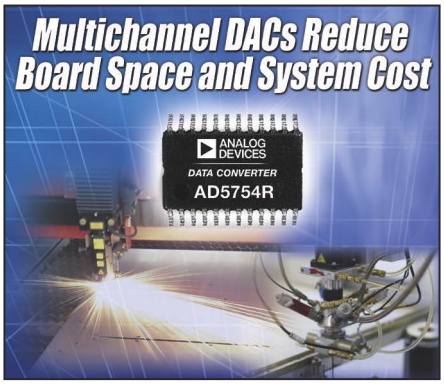

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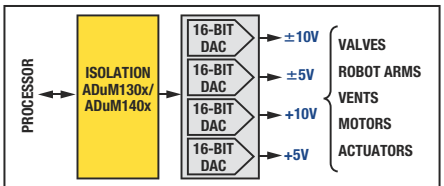

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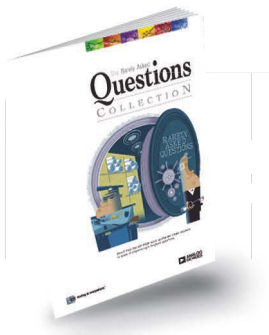


ADI Puts Software Designed Radio Within Reach via New Transmit DACs with Integrated Super-Nyquist Mixer Mode Function

With the introduction of the direct RF out mixer mode function in transmit DACs, the overall transmission subsystem moves a step closer to achieving a true software defined radio (SDR) architecture. Figure 1 below shows how a transmit DAC fits into a typical wireless transmission system. This diagram shows the traditional system where the DAC generates the desired signal within the first Nyquist zone. That signal then passes through a low-pass filter (LPF), usually called a reconstruction filter. The reconstructed analog signal is fed to the mixer stage, which upconverts and generates the RF signal at the desired carrier or IF frequency. Figure 2 below demonstrates the DAC output spectrum in mixer mode vs. normal mode, generating the RF directly, thereby eliminating the mixer and reconstruction filter.

Conceptually, operating the DAC in the mixer mode is equivalent to using a normal DAC plus LPF and mixer, but the actual implementation is not a simple integration of all components. In the traditional transmission architecture, the DAC produces a current, which flows through a load resistor to generate a voltage. The voltage goes through the LPF and is converted back to current for chopping. In mixer mode, the mixer switches and DAC switches are combined so the signal processing is more straightforward. The basic idea of the mixer mode function is shown in Figure 3. At every clock cycle, a current-steering DAC creates a current pulse whose amplitude is proportional to the input digital data word. The mixer mode function generates half-clock-cycle-wide current pulses at both rising and falling edges of the DAC clock where the output current sign is positive/negative. This mixer mode function enables synthesis of high IF and RF signals directly out of the DAC while utilizing a relatively low update rate. Figure 3 shows the difference between a DAC operating in the mixer mode and a normal DAC in frequency domain. In the case of a normal DAC, the signal of interest is located in the first Nyquist zone, with images in the second and higher Nyquist zones occurring at lower power and amplitude. With the mixer mode function enabled, the power of the images located in the second and third Nyquist zones are boosted to be the strongest ($f_{DAC} \pm f_{OUT}$) in the output spectrum. A band-pass filter can be employed to select either the upper or lower side band signal.

Some advantages of a transmit DAC operating in the mixer mode are

- Simplification of system level design and reduction in the number of components, requiring less board space.
- A higher level of transmit path integration for lower system cost and better reliability.
- Better transmit signal linearity through the elimination of the extra current-voltage-current conversions associated with external mixer stages.

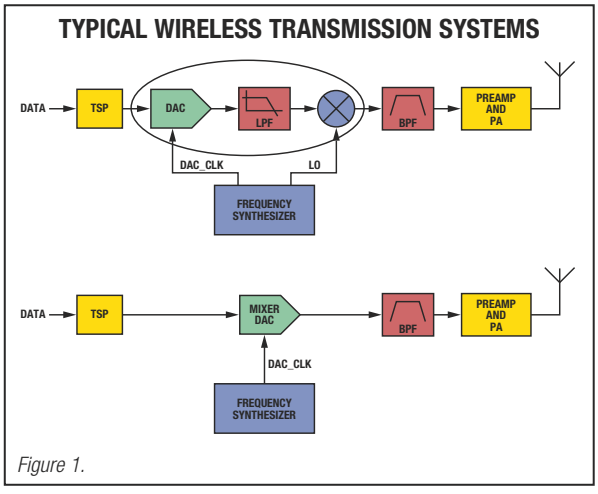


Figure 1.

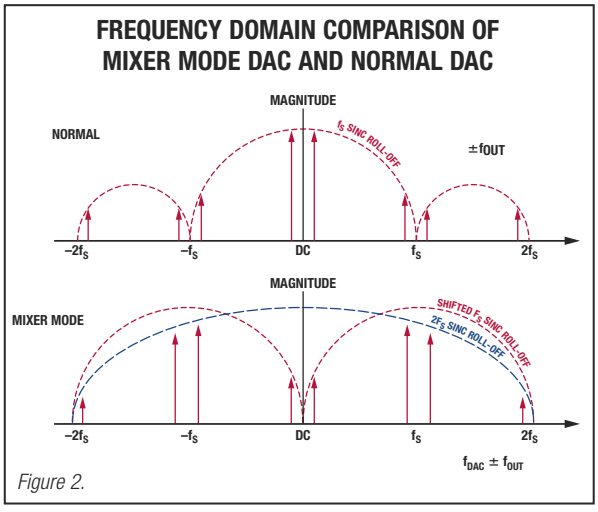


Figure 2.

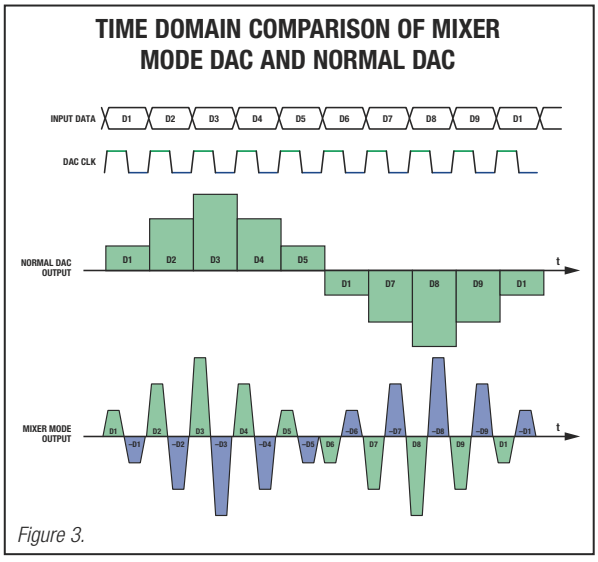


Figure 3.

Transmit DACs Selection Table

Analog Devices' portfolio of TxDAC® transmit DACs with the mixer mode functionality includes the following:

Part Number	Resolution (Bits)	Sampling Rate (MSPS)	Output Logic	Price ($U.S.)
AD9741	8	250	LVCMOS	6.49
AD9743	10	250	LVCMOS	8.11
AD9745	12	250	LVCMOS	10.13
AD9780	12	600	LVDS	16.00
AD9746	14	250	LVCMOS	13.25
AD9781	14	600	LVDS	20.00
AD9747	16	250	LVCMOS	15.90
AD9783	16	600	LVDS	22.50

*nano*DAC® Family Delivers Power and Space Savings Without Sacrificing Performance

There is a growing need for smaller industrial and communications systems, and design engineers increasingly require reduced form factors for all components. However, this reduction in component size and power cannot compromise performance. ADI addresses these needs with the *nano*DAC family of tiny-packaged DACs. The latest *nano*DAC device is the AD5664R, a 16-bit quad DAC that realizes a 70% reduction in board space over similar solutions, and also integrates an on-chip 5 ppm/°C reference. The combination of performance, integration, small footprint, and power consumption of only 5 mW at 5 V is ideal for designers of PLC cards, analog I/O boards, and many other space-constrained systems. The AD5664R is part of a family of 12-bit, 14-bit, and 16-bit pin-compatible DACs, available in both dual and quad configurations.

Part Number	Description	Max Power @ 5 V (µA)	Price ($U.S.)
AD56x4 Family, 12-Bit/14-Bit/16-Bit Quad DACs in 3 mm × 3 mm Package			
AD5664R	4-channel, 16-bit, 5 ppm/°C on-chip reference, in 10-lead MSOP and 10-lead QFN	900	10.45
AD5644R	4-channel, 14-bit, 5 ppm/°C on-chip reference, in 10-lead MSOP and 10-lead QFN	900	7.95
AD5624R	4-channel, 12-bit, 5 ppm/°C on-chip reference, in 10-lead MSOP and 10-lead QFN	900	5.99
AD5664	4-channel, 16-bit, in 10-lead MSOP and 10-lead QFN	900	9.95
AD5624	4-channel, 12-bit, in 10-lead MSOP and 10-lead QFN	900	5.49
AD56x3 Family, 12-Bit/14-Bit/16-Bit Dual DACs in 3 mm × 3 mm Package			
AD5663R	2-channel, 16-bit, 5 ppm/°C on-chip reference, LDAC, CLR, in 10-lead MSOP and 10-lead QFN	450	5.50
AD5643R	2-channel, 14-bit, 5 ppm/°C on-chip reference, LDAC, CLR, in 10-lead MSOP and 10-lead QFN	450	4.75
AD5663	2-channel, 16-bit, LDAC, CLR, in 10-lead MSOP and 10-lead QFN	450	5.05
AD5623R	2-channel, 12-bit, 5 ppm/°C on-chip reference, LDAC, CLR, in 10-lead MSOP and 10-lead QFN	450	2.49

New Direct Digital Synthesizer IC Features Programmable Modulus for Exact Frequency Tuning

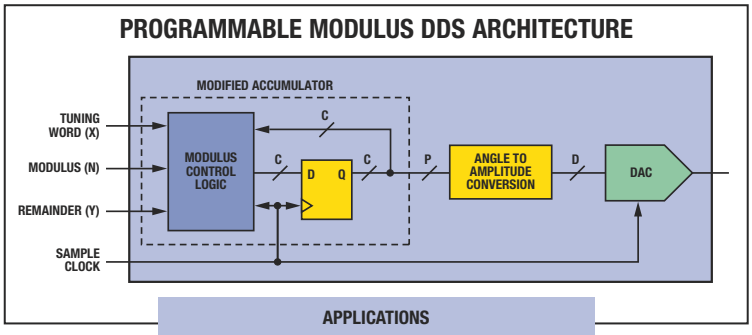
The programmable modulus function is a modification of the typical accumulator-based DDS architecture that enables DDS to be used in "any rate" applications. A typical accumulator-based DDS recursively sums the digital input tuning word at the rate of the sample clock. This produces a time series of digital words at the output of the accumulator. They increase linearly until the accumulator rolls over at its maximum value of 2^C. Hence, the accumulator output has a fixed modulus of 2^C.

The frequency of the sinusoid that appears at the DAC output for a typical accumulator-based DDS is given by the following equation:

$$f_0 = \frac{M}{2^C} f_S$$

The synthesized frequency, f_0, is a fraction of the sampling frequency, f_S, according to the rational expression, $M/2^C$, where both M and C are positive integers. The integer, M, is often referred to as the frequency tuning word. Since M, by definition, is an integer, then f_0 is constrained to the set of frequencies:

$$f_0 \in \left\{0, \frac{f_S}{2^C}, \frac{2f_S}{2^C}, \frac{3f_S}{2^C}, \ldots, \frac{2^{C-1}-1f_S}{2^C}\right\}$$



AD9913

APPLICATIONS

- Portable and handheld equipment
- Agile LO frequency synthesis
- Programmable clock generator
- FM chirp source for radar and scanning systems

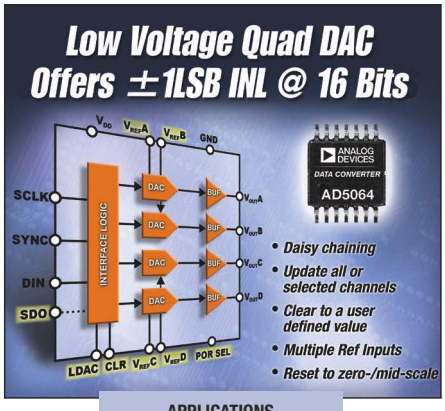
$9.65

This constrained set of frequencies prevents exact frequency tuning, which can cause problems in some applications. But what if the accumulator modulus were made adjustable? It seems reasonable to assume that an adjustable accumulator modulus would allow the use of an arbitrary integer rather than the fixed integer (2^C) in the denominator of the F_0 equation. This flexibility is exactly what the programmable modulus of the AD9913 DDS architecture offers (see figure above).

In addition to low power dissipation, the AD9913 is the first of ADI's accumulator-based DDS products to offer programmable modulus architecture. Although the underlying function of the programmable modulus technique is to alter the accumulator modulus, the actual implementation is more complicated. This complication arises from the fact the angle-to-amplitude converter must receive values that are scaled to span a full power-of-two. The AD9913 solves this problem by effectively incorporating a second accumulator. The programmable modulus function enables signal generators to be programmed to very precise frequencies, and also makes DDS a desirable option for the generation of standard network clocks. Both of these are applications that present strict requirements for frequency accuracy.

Industry's Most Accurate Low Voltage Buffered Quad DAC Offers 1 LSB INL at 16 Bits

Ideal for precision multichannel I/O systems, the AD5064 is a quad, 16-bit DAC with 16-bit accuracy over a 0 V to 5 V output span—delivering a total unadjusted error of less than ±2 mV in a compact 14-lead TSSOP package. The device is also available in 16-lead TSSOP with individual reference pins allowing each DAC the flexibility to be driven with a different reference voltage, if necessary. In addition, the device is extremely flexible and provides many convenient control features such as pin-selectable reset/power-on to midscale or zero-scale, hardware LDAC and CLR pins, and a programmable CLR function to allow the user to select clear options. Other features include LDAC override to allow only selected channels to be synchronously updated, an SDO pin to allow daisy chaining of multiple devices, and a per-channel power-down feature. Pin-compatible 12-bit and 14-bit versions are also available—ensuring easy upgrade or downgrade options.



AD5064

APPLICATIONS

- Multichannel PLC/DCS systems
- Programmable attenuators
- Gain and offset calibration

$11.50

AD5064 Features

- Resolution: 16-bit
- 1 LSB INL and DNL
- Pin-compatible: 12-bit (AD5029), 14-bit (AD5044)
- On-chip reference buffer and output amplifier
- Packaging: 14-lead, 16-lead TSSOP

Integrated Single Chip DAC IC Families with Current Output Improve Reliability and Data Quality in Process Control Equipment

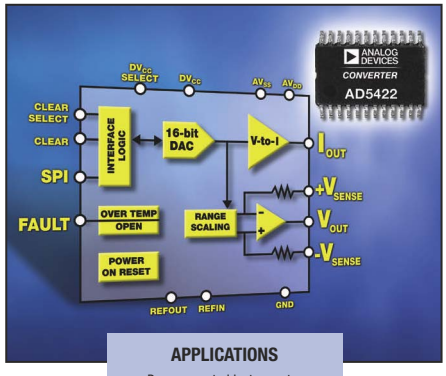
iCMOS® INDUSTRIAL

In a host of automation systems—from mining to petrochemical refinement—industrial applications require solutions to address the growing demand for robust, reliable, and high performance process control instruments. Minimal component count, operation over large temperature and supply tolerances, and performance are also key in addressing challenges in an increasingly competitive and safety conscious marketplace.

Solution

ADI leverages its over 40-year industrial market heritage to deliver the two new families of DACs that help solve these process control challenges. The AD54xx is a family of highly integrated, 12-bit and 16-bit digitally controlled current ICs. These products handle standard 4 mA to 20 mA data transmission and diagnostic requirements with user-programmable current mode output configurations, eliminating bulky discrete analog drive and fault detect circuitry—thereby increasing the reliability of the system.

Enabled by ADI's proprietary *i*CMOS® manufacturing process technology, the AD5420 features software-selectable current output ranges of 4 mA to 20 mA, 0 mA to 20 mA, or 0 mA to 24 mA. The device operates from single-supply voltages of 10.8 V to 60 V to facilitate reliable factory communications over large cabling distances. Analog outputs can drive resistive loads up to 1.5 kΩ and inductive loads of 1 H. The AD5420 boasts 0.1% TUE (total unadjusted error), 5 ppm/°C output error drift, and only 0.01% linearity. Internal fault detection circuitry provides hardware and software indication of system faults such as opens in cable wiring or overtemperature conditions. The part also integrates a digital slew rate control feature to reduce the rate of change of the output in systems with large cabling and an asynchronous CLEAR pin for output control during power-up/power-down conditions. The flexible serial interface is SPI and MICROWIRE compatible and can be operated in 3-wire mode to minimize the digital isolation required in isolated systems. The AD5410 is a pin-compatible, 12-bit device.



APPLICATIONS
- Process control instruments
- Distributed control systems
- 4 mA to 20 mA transmitters

Current Source and Voltage Output DACs

The AD5422 and AD5412 are, respectively, 16-bit and 12-bit current source and voltage output DACs and operate from a single 12 V to 48 V supply, or dual ±12 V to ±24 V supplies. All devices in the AD54xx family integrate a precision 5 ppm/°C reference and are specified over the extended industrial temperature range of –40°C to +105°C. Both are available in LFCSP and TSSOP packaging.

AD5420 Features

- Resolution: 16-bit
- Current output: 0.1% TUE
- Drive capability: 1.5 kΩ, 1 H
- Integrated 5 ppm/°C reference
- On-chip fault detection
- Asynchronous output control
- Package: 24-lead TSSOP, 6 mm × 6 mm LFCSP

Part Number	Resolution/Configuration	Compliance (V)	Accuracy (TUE)	Price ($U.S.)
AD5422	16-bit, 4 mA to 20 mA current source and voltage output DAC	±12 to ±24, 10.8 to 40	0.1%	4.95
AD5412	12-bit, 4 mA to 20 mA current source and voltage output DAC	±12 to ±24, 10.8 to 40	0.3%	3.79
AD5420	16-bit, 4 mA to 20 mA current source DAC	10.8 to 60	0.1%	4.32
AD5410	12-bit, 4 mA to 20 mA current source DAC	10.8 to 60	0.3%	3.35

Online Seminar Series

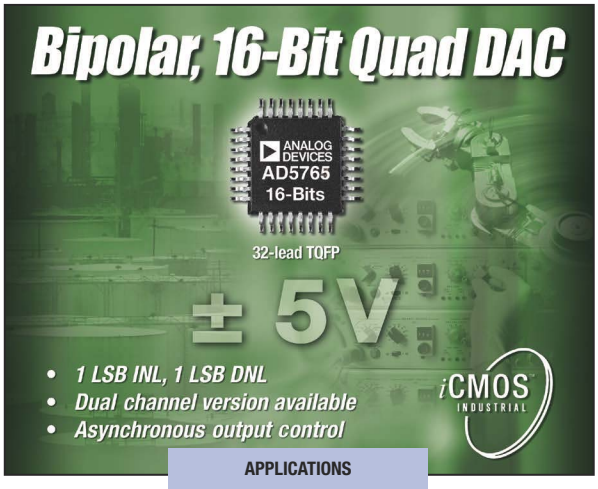
"Data Conversion Applications and Solutions for Precision Process Control" at *www.analog.com/onlineseminars*.

For samples and data sheets, visit www.analog.com/V8DAC

ANALOG DEVICES

Industry's Highest Performance Quad ±5 V Digital-to-Analog Converter

The AD5765 DAC offers a significant step forward for makers of measurement and data acquisition equipment for which full 16-bit performance, high integration, and small footprint are important requirements. The introduction of the AD5765 means that designers no longer have to spend time compensating for unwanted effects in the system, making the design task easier and more efficient. Enabled by ADI's *i*CMOS technology, the AD5765 achieves a threefold improvement in accuracy over previously available high voltage DACs while using 50% less board space. This ±5 V, quad, serial input, bipolar voltage output DAC features 16-bit resolution, 1 LSB INL, 1 LSB DNL, and gain and offset calibration of less than 1 mV. In addition, the device integrates features essential to reducing design time and overall system cost. The features include an on-chip reference buffer, low headroom/wide swing amplifier, power-on reset, power-on/power-off output control, and I/O lines. The AD5765 is ideal for both closed-loop servo control and open-loop control applications. The AD5765 is available in a 32-lead TQFP and offers guaranteed specifications over the –40°C to +85°C industrial temperature range. Also available are a dual channel version (AD5763), as well as 14-bit and 16-bit versions with integrated references.



Part Number	Description	Number of DACs	Supply (V)	Price ($U.S.)
AD5765	16-bit, 1 LSB DAC	4	±5	16.50
AD5763	16-bit, 1 LSB DAC	2	±5	11.40
AD5764R*	16-bit, 1 LSB DAC	4	±15	27.50
AD5762R*	16-bit, 1 LSB DAC	2	±15	16.80
AD5744R*	14-bit, 1 LSB DAC	4	±15	23.60

*(R) denotes integrated precision 10 ppm (max) reference.

Quad Channel, 256-Position Digital Potentiometers Reduce Board Space and Provide Design Flexibility

Multichannel digital potentiometers not only save board area but provide design flexibility as each channel can be configured as a variable resistor (rheostat) or as a voltage divider (DAC) allowing a single device to solve multiple design challenges. The AD5204 is a multichannel device that provides four 256-position digital potentiometers in a space-saving 5 mm × 5 mm QFN package.

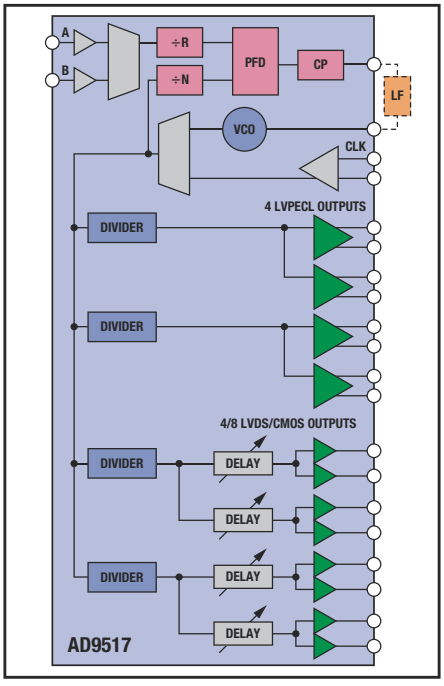
Analog Devices provides a broad family of multichannel digital potentiometers offering different interfaces, resolutions, and memory options.

Part Number	Number of Channels	Number of Positions	Memory Type	Interface	Resistor Values (kΩ)	Voltage Range (V)	Temperature Range (°C)	Price ($U.S.)
AD5203	4	64	Volatile	SPI	10, 100	5.5	–40 to +85	1.45
AD5204	4	256	Volatile	SPI	10, 50, 100	±3, 5.5	–40 to +85	1.50
AD8403	4	256	Volatile	SPI	1, 10, 50, 100	5.5	–40 to +125	2.76
AD5263	4	256	Volatile	SPI, I²C®	20, 50, 200	±5, 15	–40 to +125	2.55
AD5206	6	256	Volatile	SPI	10, 50, 100	±3, 5.5	–40 to +85	1.92
AD5233	4	64	Nonvolatile	SPI	1, 10, 50, 100	±3, 5.5	–40 to +85	2.47
AD5253	4	64	Nonvolatile	I²C	1, 10, 50, 100	±3, 5.5	–40 to +85	2.46
AD5254	4	256	Nonvolatile	I²C	1, 10, 50, 100	±3, 5.5	–40 to +85	2.55

Multioutput Clock Generators Improve System Reliability and Reduce Costs

ADI's AD9517-x series of low phase noise multioutput clock generators provides all critical timing functions on a single IC and at jitter levels less than 500 fs (femtoseconds) rms. These products reduce BOM costs, board space, and eliminate the reliability issues of standalone VCOs by integrating a PLL synthesizer, two reference inputs, a VCO, programmable dividers, adjustable delay lines, and clock drivers replacing multiple discrete components. The selectable logic and flexible frequency output combinations are perfect for clocking multiple system components, including DACs, ADCs, FPGAs, and others.

Following the success of the AD9516-x, the AD9517-x and AD9518-x derivatives are now available in a smaller packages and with different output channel variations. To further meet customer needs, five versions of each device are available to support multiple VCO tuning ranges from 1.45 GHz to 2.95 GHz.



Part Number	Outputs	Dividers	Delay Lines	Package	Price ($U.S.)
AD9516-x	6 LVPECL, selectable 4 LVDS or 8 CMOS	5	4	64-lead LFCSP, 9 mm × 9 mm	12.50
AD9517-x	4 LVPECL, selectable 4 LVDS or 8 CMOS	4	4	48-lead LFCSP, 7 mm × 7 mm	11.40
AD9518-x	6 LVPECL	3	None	48-lead LFCSP, 7 mm × 7 mm	9.85

Low Jitter Clock Buffers Improve Data Converter Performance

Today's high speed, high performance data converters are able to sample very high frequency signals with great accuracy. To do so reliably, however, requires an extremely low jitter clock source driving the converter's clocking input pins. With growing demand for increased system speed and precision, it is no longer realistic to rely on a single centralized clock source—that is passively routed on a printed circuit board—to deliver a sufficiently low jitter clock to data converter stages. ADI's new family of low jitter clock buffers, when situated in the clock tree scheme, solves this problem by delivering a strong, clean clock signal throughout the system. This buffering function optimizes converter performance and signal fidelity for high performance applications such as communications, digital imaging, and other equipment that processes real-world analog signals. ADI's family of clock buffers delivers fast edges and contributes less than 60 fs of additional jitter.

APPLICATIONS

- Clock and data signal restoration and level shifting
- Data converter clocking
- Automated test equipment (ATE)
- High speed instrumentation

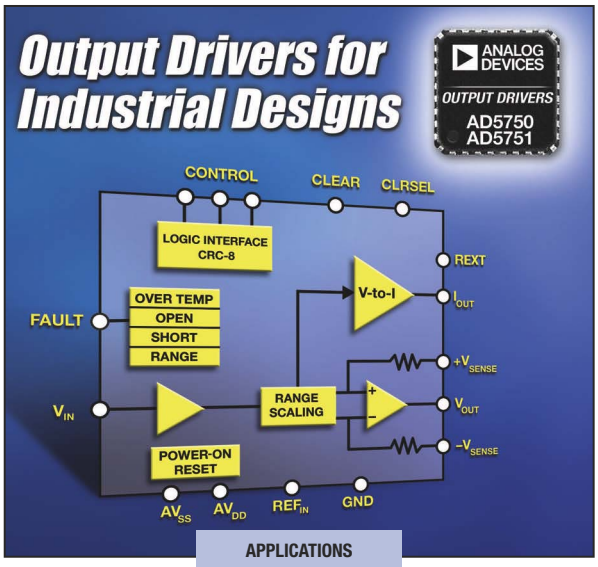
"Performance Clocks: Demystifying Jitter" is available at *www.analog.com/onlineseminars*.

Part Number	Number of Inputs	Number of Outputs	Max Clock Input (GHz)	Output Logic	Wideband Random Jitter (ps rms)	Price ($U.S.)
ADCLK905	1	1	6	ECL, PECL, LVPECL	0.06	5.60
ADCLK907	2	2	6	ECL, PECL, LVPECL	0.06	6.75
ADCLK914	1	1	6	High voltage differential signaling (HVDS)	0.1	6.95
ADCLK925	1	2	6	ECL, PECL, LVPECL	0.06	5.95

Introducing the Industry's Most Accurate Voltage/Current Output Driver for Industrial Control Systems

The AD5750 and AD5751 are single channel, high performance, voltage/current output drivers with hardware- or software-programmable output ranges. The AD5750 operates from industry-standard ±12 V to ±24 V supplies and delivers 5 ppm/°C output drift, 0.01% linearity, and 0.1% TUE (total unadjusted error). The output configuration is software-selectable from options of 5 V, 10 V, ±5 V, and ±10 V in voltage mode and 4 mA to 20 mA, 0 mA to 20 mA, 0 mA to 24 mA, and ±20 mA and ±24 mA in current mode. All output spans include an additional overrange setting.

Analog outputs are short-circuit and open-circuit protected and can drive capacitive loads of 1 μF and inductive loads of 0.1 H. The AD5750 integrates packet error checking (PEC) to verify that interface data has been correctly received in the presence of noise—useful in industrial environments where data communications corruption can occur. The device also includes an asynchronous CLEAR pin that sets the outputs to zero-scale/midscale in voltage mode or the low end of the selected current range in current mode. The AD5751 operates with single supplies of 12 V to 60 V and features unipolar voltage and current mode output configurations. Both devices are specified over the –40°C to +105°C extended industrial temperature range and are housed in a 5 mm × 5 mm LFCSP package. Chip fabrication is on ADI's *i*CMOS process technology.



APPLICATIONS

- PLC/DCS systems
- Actuator control
- Data acquisition systems

AD5750/AD5751 Features

- Software-programmable V/I outputs
- On-chip diagnostics
- 0.1% TUE
- 5 ppm/°C output drift
- Asynchronous output control
- Package: 32-lead, 5 mm × 5 mm LFCSP

AD5750	$2.45
AD5751	$3.02

Analog Devices, Inc. Worldwide Headquarters
Analog Devices, Inc.
One Technology Way
P.O. Box 9106
Norwood, MA 02062-9106
U.S.A.
Tel: 781.329.4700
(800.262.5643,
U.S.A. only)
Fax: 781.461.3113

Analog Devices, Inc. Europe Headquarters
Wilhelm-Wagenfeld-Str. 6
80807 Munich
Germany
Tel: 49.89.76903.0
Fax: 49.89.76903.157

Analog Devices, Inc. Japan Headquarters
Analog Devices, KK
New Pier Takeshiba
South Tower Building
1-16-1 Kaigan, Minato-ku,
Tokyo, 105-6891
Japan
Tel: 813.5402.8200
Fax: 813.5402.1064

Analog Devices, Inc. Southeast Asia Headquarters
Analog Devices
22/F One Corporate Avenue
222 Hu Bin Road
Shanghai, 200021
China
Tel: 86.21.2320.8000
Fax: 86.21.2320.8222

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The megapixel race: a chip designer's point of view

AS CMOS IMAGE SENSORS HAVE MIGRATED FROM LOW-END APPLICATIONS TO MULTIMEGAPIXEL CAMERAS, EMPHASIS HAS SHIFTED FROM INTEGRATING DIGITAL CIRCUITS TO THE FUNDAMENTAL DESIGN OF THE PIXEL ITSELF.

During the operating, or integration, mode, visible photons generate electrons in the pixel cell of a CMOS image sensor. The pixel collects the electrons and then translates the accumulated charge to voltage signals that serve as an output. Expressing this process quantitatively, pixel responsivity is the relation between the electrical signal and its exposure to light (V/lux×sec). "Full-well capacity" is the number of electrons that the pixel can collect. Dynamic range is roughly the number of resolvable gray levels, which you calculate by dividing the maximum signal by the minimum detectable signal and usually report in decibels.

Thermally generated electrons are obviously enemies of image sensors, because the pixel collects them along with optically generated electrons; they steal well capacity and add noise. Thus, the rate of the electrons' thermal generation within the pixel, or "dark current," is a major performance measurement that you generally report in electrons per second. Pixel development requires simultaneous optimization of all of the above parameters, along with a few additional ones—a major challenge within the world of pixel design.

Inside each pixel are a light-sensitive diode and at least three transistors. As resolution increases, transistors must be very small to allow as much area as possible where the diode can collect light. That necessity requires advanced CMOS processes. But in processes of 180 nm or less, transistors need strong well implants and shallow source-and-drain implants that cause higher junction leakage and eventually increase the dark current in the CMOS pixel array. Also, STI (shallow-trench isolation) between the transistors causes stress and increases the number of defects within the silicon, which again gives rise to higher dark current. To understand the complexity of this problem, explore the operation of a pixel and then look at optimizations.

OPERATING PRINCIPLES

Figure 1 shows a pixel with three transistors and a photo diode. A photon hits the silicon, generating an electron and a hole. This electron-hole pair travels together in the silicon until it encounters an electric field, in which the electron moves toward the higher voltage, and the hole migrates to ground. Within the CMOS pixel, a photo diode—usually

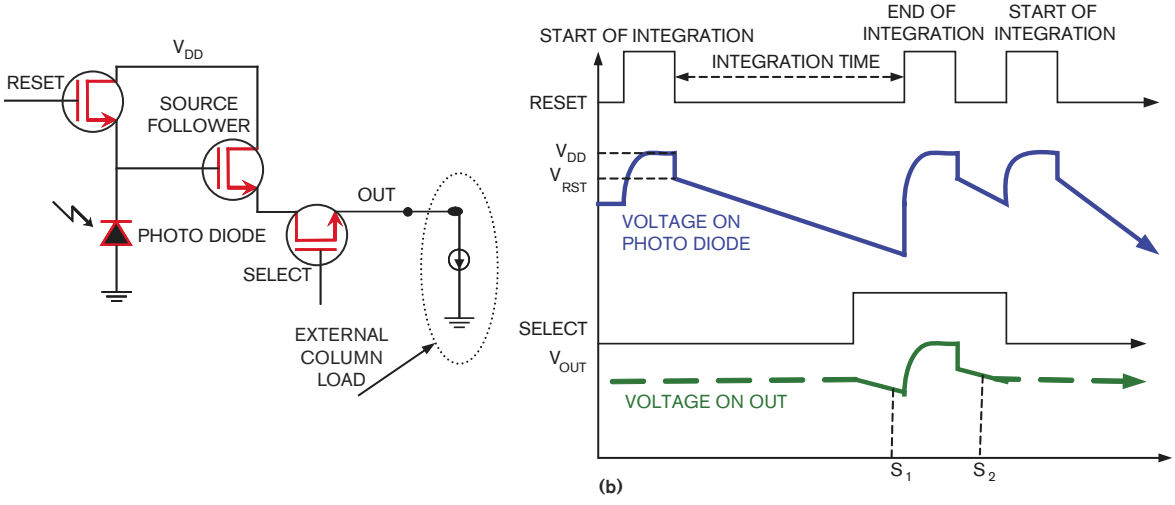


Figure 1 A typical CMOS pixel has three transistors and a photo diode (a). Typical "rolling-shutter" timing samples the signal twice (b).

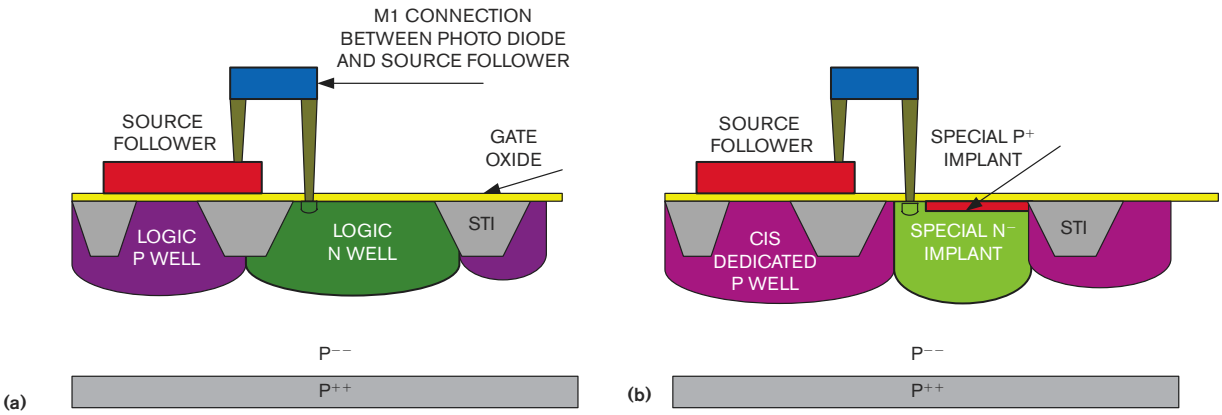
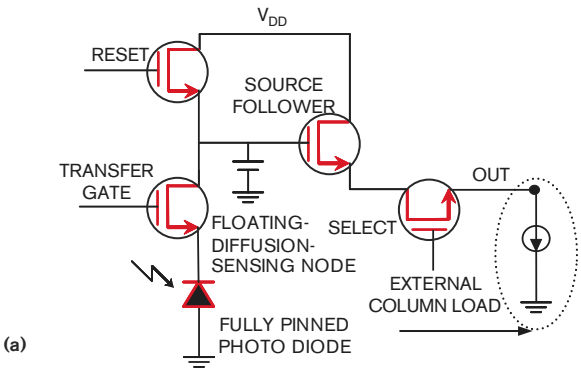
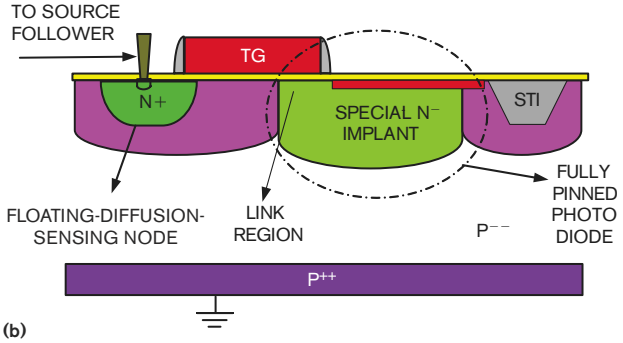


Figure 2 A cross-section of a typical CMOS-image-sensor front end adds no process steps on top of the plain-vanilla CMOS (a). A state-of-the-art CMOS-image-sensor front end adds three front-end-process steps (b).





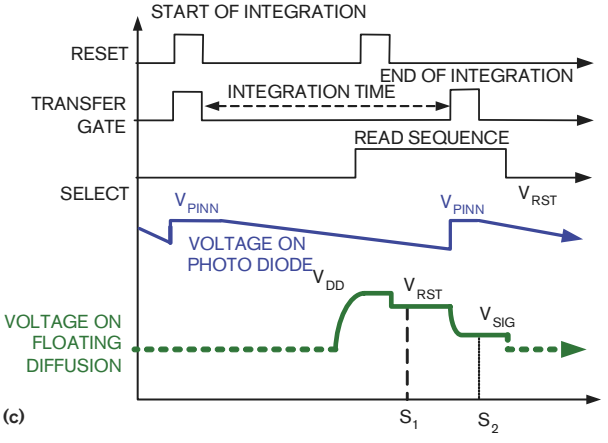


Figure 3 An electrical diagram of a four-transistor pixel has a fully pinned photo diode (a) that you can view in cross-section along with the transfer-gate transistor (b). In a typical timing diagram for a four-transistor pixel, the integration starts by activating the reset and transfer-gate transistors and setting the diode to its pinned potential (c).

an N-type implant in a P-type region—generates the separating electric field.

The photo electrons accumulate in the diode and cause a drop in voltage that is proportional to their number. The number of photo electrons is, in turn, proportional to the photon flux. Thus, the voltage drop in the diode is proportional to the photon flux. To increase this signal pixel, designers employ quantum efficiency—increasing the number of electrons for a given photon flux. They also try to increase the voltage drop on the diode for a given charge. This value is the "pixel-conversion gain," and it is inversely proportional to the photo diode's capacitance.

You optimize the quantum efficiency of a photo diode by engineering it so that its electric field penetrates deeply into the silicon. This step is important for photons in the green-to-red spectrum, because photons with longer wavelengths tend to penetrate deeper into the silicon. It helps to replace the standard starting material with low-doped, P-type epitaxial material grown on P^{++} substrate.

In the first generation of the three-transistor pixel, designers made the diode by implanting the regular PMOS N well into the P^{--} substrate (**Figure 2a**). Another common approach was to use the N^{++} of the NMOS-transistor source-and-drain implant. Although these options are fully compatible with the regular CMOS process, the resulting diode exhibits poor performance. For example, using a large N-well diode, which you need for good collection of photo electrons, causes the pixel capacitance to be excessive. Thus, the overall efficiency of translating photon flux to voltage drops becomes lower than necessary.

Another serious problem with diodes that are based on CMOS implants is their typical dark current. Dark current af-

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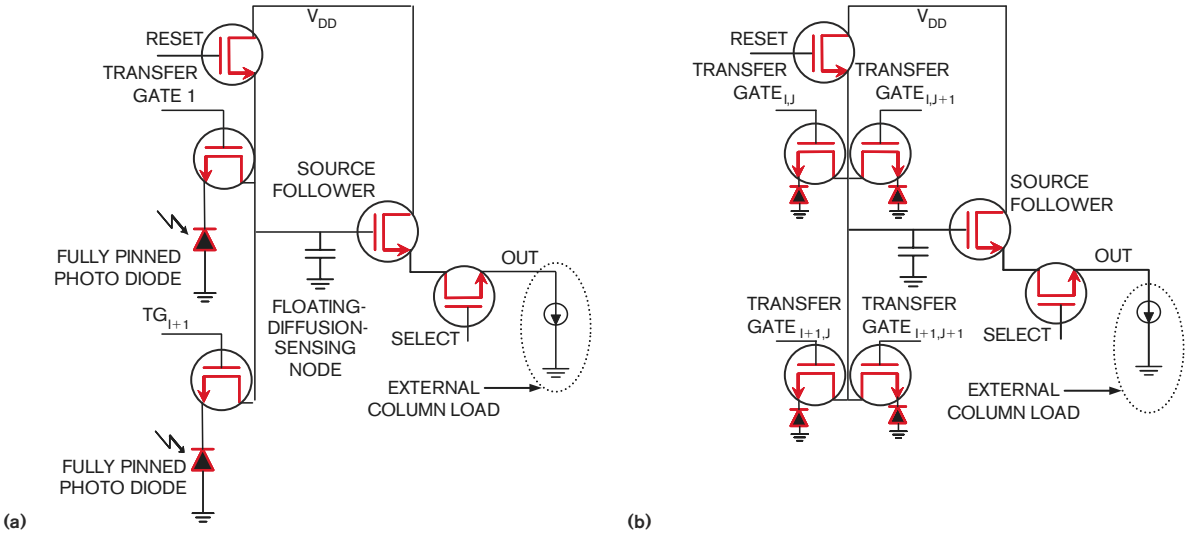

Figure 4 An electrical diagram of a two-shared configuration uses mature pinned-photo-diode technology, arranging the photo diodes and their associated transfer-gate rows. There is one reset, one select, and one source-follower transistor for each group of pixels in two consecutive rows (a). A four-shared configuration uses mature pinned-photo-diode technology, arranging the photo diodes and their associated transfer gates in a 2×2 configuration. There is one reset, one select, and one source-follower transistor for each group of pixels in two consecutive columns and rows (b).

fects the noise floor of the pixel and thus determines the low level of illumination a pixel can integrate and still have meaningful data. For good image quality, it must be smaller than 100e/sec per pixel, where e is electrons. You can set much lower and more aggressive values than the in-room temperature to ensure that the dark current does not deteriorate the image quality—even at 60°C. The dark current depends on several factors: the diode temperature, the number of silicon defects near the diode's electric field, and the electric-field strength.

Because regular CMOS implants are not optimized for low leakage, they usually exhibit a dark current of approximately 1000e/sec for the N-well implant (one order of magnitude higher than needed) and even higher for a source-and-drain implant. The situation is even worse, because the N^{++} implants induce defects in the surrounding silicon. The implant anneal typically cures these defects, but, when you try to manufacture several-megapixel arrays, some of the N^{++} diodes have significantly higher dark current than the average. Such pixels with excessive dark current appear in a black picture as twinkling or shining stars. Because our eyes are immediately drawn to high-frequency perturbation in the image, these leaky pixels ruin the overall image quality; if they cluster together, they make the entire chip unusable.

THE PIXEL TRANSISTORS

The role of the source-follower transistor in the pixel is to decouple the photo diode from all other pixels that connect to the same column-output line. When the row-select transistor is open, the column-current source maintains a few microamps in the source-follower transistor. In theory, the source-follower transistor will support this current as long as the voltage at its source is $V_S=G_{SF}\times V_{PD}-V_{TRSF}$, and $V_{PD}>V_{TRSF}$, where G_{SF} is the source-follower gain, V_{PD} is the photo-diode voltage, and V_{TRSF} is the source-follower threshold voltage. In an ideal case, V_S is linear with V_{PD}. However, in a typical logic transistor V_{TRSF} increases with V_S, making the first equation highly nonlinear and reducing the dynamic range of the pixel. A common approach to this problem is to replace the P-well implants of the logic transistors with a carefully designed new P well that makes the source-follower transistor immune to this effect.

Figure 2 illustrates a first-generation three-transistor pixel with no additional masks, compared with a state-of-the-art pixel requiring three additional masks. You use the first mask for a special photo-diode N^- implant, which gives the exact capacitance for a given pixel design. The second mask is a P^+ mask that prevents electric fields from reaching the surface, significantly reducing the dark current. Notice that, because in a three-transistor design, you need to directly connect the photo diode and source-follower transistor, the P^+ implant does not cover a small region near the diode's contact. This diode is partially buried. The P^+ implant also creates another separation field near the diode surface, which helps to increase the quantum efficiency for blue photons.

The third mask reduces the body effect of the source-follower transistor, making its threshold voltage immune to changes in source voltage. These changes apply only in the pixel array; the array periphery, including controls, ADCs, and DSP, still uses the well-established and optimized logic-CMOS process.

The main problem that makes the three-transistor pixel unusable for small pixels is that, as the number of photons available for collection decreases, the signal decreases. To maintain the same SNR (signal-to-noise ratio), you must suppress noise sources.

The main noise source in dark areas, once you suppress the dark current, is the so-called reset noise. Referring back to **Figure 1b**, you begin integration by setting the photo diode to high voltage by pulsing the reset transistor. When the re-

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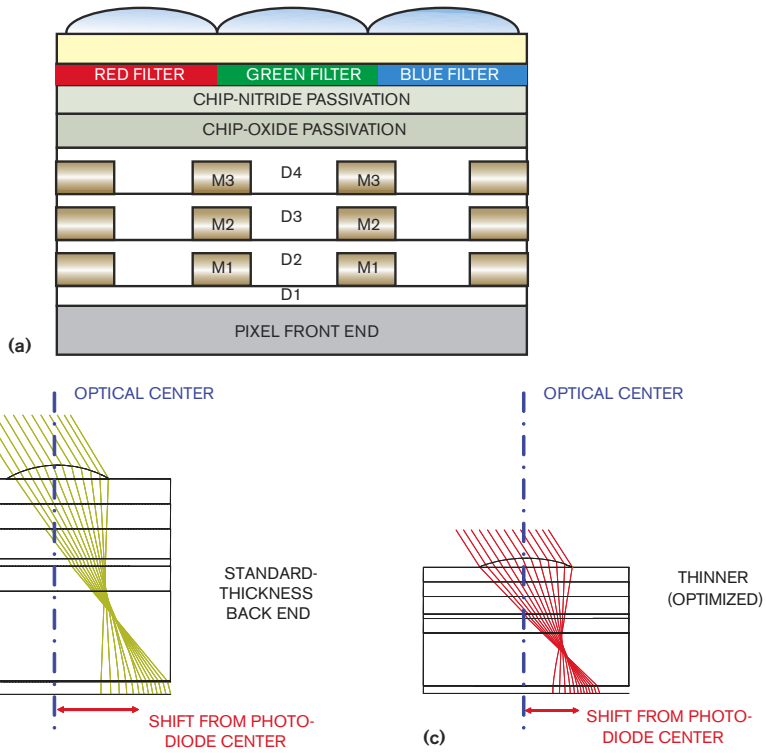

Figure 5 A typical CMOS image sensor uses three metal layers inside the pixel and four layers of metal in the periphery (a). The angle of incidence of light depends on the pixel's location in the array—whether for a standard CMOS back end (b) or an optimized CMOS-image-sensor back end (c).

set transistor returns to idle, the diode starts collecting photons, and its voltage decreases. At the end of the integration time (S_1), the output voltage copies to an analog memory in the column circuit. Again pulsing the reset gate sets the diode to high voltage, which copies to another analog memory (S_2) in the column amplifier.

The photon flux is theoretically proportional to the difference between these two voltages that the analog memory stores. But, because the start-of-integration-reset event and the read-reset event can't be simultaneous, the sample of diode high voltage that the system sends to the column amplifier is not exactly equal to the diode voltage at the beginning of integration, significantly contributing to noise. The common way to eliminate this noise is to use a four-transistor pixel and a fully pinned photo diode.

THE FOUR-TRANSISTOR PIXEL

Figure 3a shows a four-transistor CMOS-image-sensor pixel, including a fully pinned photo diode. The fully pinned diode has relatively small free-charge capacity. The construction of the diode is similar to that of the partially buried photo diode in **Figure 2b** but with one significant change: There is no contact between the photo diode and source-follower transistor, virtually eliminating the surface contribution to dark current.

With a fully pinned and properly designed photo diode, all free electrons from the diode flow out when the reset and transfer-gate transistors are active. In that case, the potential in the diode reaches its minimum value—the pinned potential, which it reaches repeatedly every time you evacuate all electrons from the diode. This feature enables noise reduction and is the main advantage of the fully pinned photo diode over conventional diodes.

Figure 3c illustrates proper four-transistor-pixel operation. The integration starts by activating the reset and transfer-gate transistors and setting the diode to its pinned potential. After integration, the reset transistor activates and sets the floating-diffusion capacitor to high voltage and copies this voltage to the first

memory bank at the column circuit. Opening the transfer-gate transistor then transfers the photo electrons to the floating-diffusion capacitor. The resulting voltage of the capacitor then copies to the second memory bank at the column circuit. You calculate the photo signal by subtracting the signal voltage from the reset voltage. Although the reset voltage is noisy because its value fluctuates every time you reset the floating-diffusion capacitor, the photo signal itself is noise-free, as long as you get all electrons in the photo diode into the capacitor.

To ensure low-noise operation, this cycle must collect all the electrons from the diode through the link region between the diode and the transfer gate. This task is the main optimization duty for a four-transistor pixel. Pixel designers do this optimization by changing the layout and the implant. This scheme is not scalable in any way, and you have to start almost from scratch for each new pixel-size design.

Another optimization of a typical four-transistor design is the reduction in temporal noise of the source-follower transistor, which becomes dominant when you've eliminated other sources. The transistor noise is mainly due to defects in its gate oxide and on the shallow-trench-isolation interface with silicon. To reduce or eliminate these defects, you must open the most difficult process modules in a given CMOS-process node and reoptimize them. But, as pixels become smaller, this activity becomes inevitable to keep SNR constant.

FURTHER OPTIMIZATION

One way of retaining both a big diode and a big optical opening in a small pixel is to share several photo diodes and their associated transfer gates with one floating-diffusion capacitor, one reset transistor, one source-follower transistor, and one row-select transistor. **Figure 4a** shows a "two-shared" pixel. In this example, there are five transistors on two photo diodes, resulting in 2.5 transistors per diode, an even better ratio than that of the three-transistor pixel. This configuration is beneficial for pixels larger than 2.5 microns. For smaller pixels, a "four-shared" configuration with only 1.75 transistors per photo diode is common (**Figure 4b**). Although it seems attractive to increase the number of shared photo diodes and hence to decrease the photo-insensitive area, there is a physical limit to doing so. The floating-diffusion capacitance tends to increase linearly with the number of shared transfer gates, causing a decrease in pixel responsiveness.

THE OPTICAL STACK

You know how to modify the pixel front end of an ordinary CMOS process to increase response and reduce pixel noise. In parallel, innovative efforts are under way to optimize the pixel's optical stack, thus improving the optical path to the silicon.

Figure 5a shows the typical back-end scheme of a CMOS image sensor. A typical CMOS image sensor uses three metal layers inside the pixel and four layers of metal in the periphery. The passivation layer typically comprises oxide and nitride and resides above the last interdielectric layer—D4 in the case of the four-level metal stacks. The red, green, and blue polymeric filters, which are responsible for the color reproduction of the images, reside above the passivation layer. (A single pixel without a color filter can provide only monochrome information.) The microlens that directs the light into the photodiode resides above the color filter.

The microlens must cover most of the pixel area to gather even the light that impinges on the periphery of the pixel. However, producing the microlenses with no space between them is difficult and usually results in some photo-response nonuniformity: the main noise source in medium to high illuminations. Second, you must determine the height of the microlens. Here, you choose a focus point between M1 and M2 of the pixel. Because the focus point is a function of microlens curvature, itself a function of pixel size, microlens space, and microlens height, pixel designers must repeat the optimization of the focus point for each reduction of pixel size.

The angle of incidence of light depends on the pixel's location in the array. The pixels near the edges of the array get most of their light at some angle to the optical axis, so the focus point for these pixels is not in the center of the pixel. The shift depends heavily on the height of the total stack between the microlens and the silicon surface (**Figure 5b**).

Two improvements can help. Designers can shift the optical axis of the mi-

crolens at the center of the photo diode within the middle of the array by the needed amount to direct angled rays to the diode's center. This operation is simple, but it requires good simulation tools and knowledge of the lens system of the final camera. Designers can also reduce the stack height by decreasing the metal and interdielectric thicknesses. This task is complicated and, by definition, changes major characteristics of the baseline-CMOS process. It also requires additional qualification of the technology. The change is so far-reaching that some of the CMOS modules in the periphery require redesign.

Some CMOS-image-sensor companies have recently moved to copper back-end processes. For copper, the interdielectric layers comprise layers of oxide and nitride. Because this structure is built exactly like an interference filter, some of the visible spectrum photons cannot reach the surface, making a copper CMOS back end unsuitable for image sensors. The main reason to move to a copper-back-end process is the availability of fine-lithography features with CMOS technology based on copper. To adapt this advanced fabrication technique to CMOS image sensors, a special process replaces the nitride layers in the interdielectric with oxide.

Bringing the light from the chip surface to the diode is one of the biggest unsolved tasks for pixels of less than 1 micron. Companies are trying to implement radical changes into their processes to design even smaller pixels. Consider the back-side-illumination scheme, which companies base on photons coming from the back side of the silicon—to the pixel—without encountering the pixel-metallization layers. A different yet novel approach is to use a wave-guiding scheme, which you base on the creation of miniature structures above each pixel to guide the light from the surface of the chip to the diode.

Achieving good CMOS-image-sensor performance is a complex task. However, scientists and engineers are trying new and inventive ideas that will no doubt produce clearer and crisper images using increasingly smaller pixels in megapixel-image-sensor arrays. EDN

AUTHORS' BIOGRAPHIES

Assaf Lahav is chief pixel designer for the CMOS-image-sensor R&D group at Tower Semiconductor, where he serves as lead engineer, developing advanced pixels, mainly for cellular-phone applications, and working on high-end imaging arrays. He holds bachelor's, master's, and doctorate degrees from Technion, Israel Institute of Technology (Haifa).

Amos Fenigstein holds bachelor's, master's, and doctorate degrees from Technion, Israel Institute of Technology (Haifa). He worked with SCD on the state-of-the-art MCT for infrared-image sensors until 1998. From 1998 to 2001, Fenigstein was with Intel, managing a failure-analysis team. Since 2001, he has been with Tower Semiconductor, serving as director of R&D for CMOS image sensors and the company's nonvolatile memory-product line.

LINEAR TECHNOLOGY

DESIGN NOTES

Step-Down Synchronous Controller Operates from Inputs Down to 2.2V

Design Note 443

Wei Gu

Introduction

Many telecommunications and computing applications need high efficiency step-down DC/DC converters that can operate from a very low input voltage. The high output power synchronous controller LT3740 is ideal for these applications, converting input supplies ranging from 2.2V to 22V to outputs as low as 0.8V with load currents from 2A to 20A. Applications include distributed power systems, point-of-load regulation and conversion of logic supplies.

A major challenge in designing a step-down converter with low V_{IN} is that the gate voltage for the N-channel MOSFETs is not readily available. The LT3740 solves this problem by integrating a DC/DC step-up converter for generating its own MOSFET gate drive voltage with a small inexpensive external inductor. This function permits the use of inexpensive off-the-shelf 5V gate-drive MOSFETs, offering up to 3% higher efficiency than sub-logic gate-drive MOSFETs and eliminating the need for a secondary supply.

The LT3740 operates at a fixed 300kHz frequency and employs valley current mode control to deliver excellent transient response and very low on-times. Furthermore, a power good signal is available to monitor the output voltage. The tracking capability built into XFER can be used to implement control of the output voltage when ramping up and ramping down. If less than 0.8V is applied to XFER, the LT3740 uses this voltage as its reference for regulation.

"Dying Gasp" Applications

The LT3740's low V_{IN} feature makes it a good fit in "dying gasp" applications for high reliability computers. In these systems, when the power gets cut, a large bank of electrolytic capacitors at the input charged to 12V or so, serve as input to the power controller. The LT3740 can operate down to 2.2V, which allows it to run longer from the input capacitors' charged voltage than a controller requiring a higher input voltage. This effectively reduces the input capacitance requirements, which can save significant board space.

Figure 1 shows a typical application circuit. The LT3740 circuit, after its input power gets cut, is able to supply the

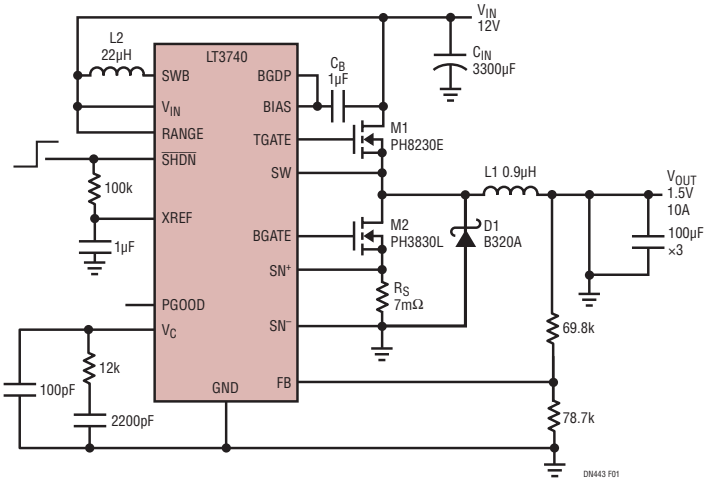

Figure 1. "Dying Gasp" Application Circuit

load for 40ms as shown in Figure 2. In comparison, the output voltage would drop out after 25ms with a controller that shuts down when the input reaches 7V.

Generate a Negative Voltage from a Low Positive V_{IN}

Figure 3 shows a 2.4V to 14V input to –3.3V at 3A output converter. The LT3740 works particularly well in this application due to its wide input voltage range and ability to operate down to 2.2V. The LT3740 also operates with synchronous rectification, which allows the use of high efficiency MOSFETs, instead of less efficient switching diodes.

Wide Input Voltage Range

The LT3740 offers high efficiency over a wide input voltage range (2.2V to 22V) and produces output voltages as low as 0.8V. The LT3740 employs valley current mode control to deliver excellent transient response and very low on-times. Figure 4 illustrates low duty cycle waveforms for a 22V input, 0.8V output application at a fixed frequency of 300kHz.

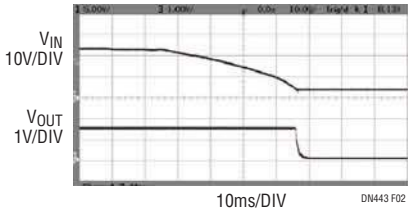

Figure 2. Input and Output Voltages Waveforms When Input Power is Removed

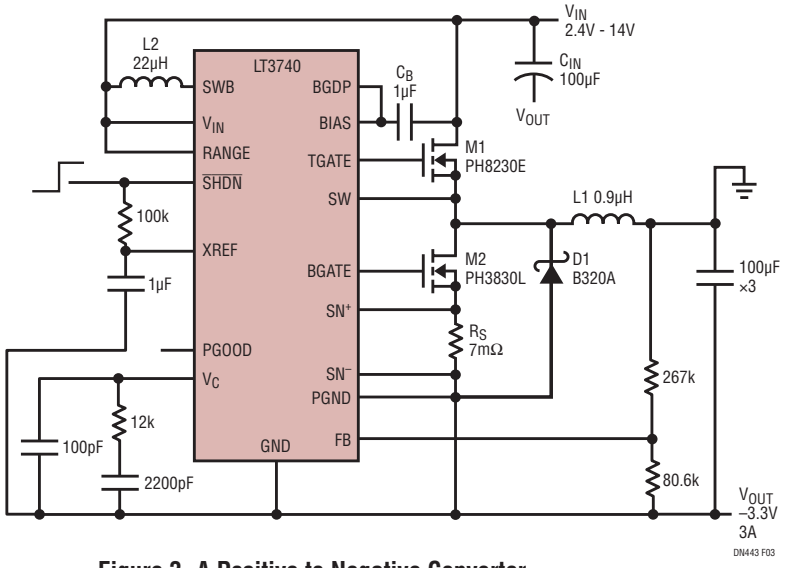

Figure 3. A Positive to Negative Converter

Conclusion

The LT3740 can operate from low input voltages, providing a space- and cost-saving solution over a wide input voltage range. The LT3740 is a versatile platform on which to build DC/DC converter solutions that use few external components and maintain high efficiencies over wide load ranges. The integrated step-up regulator facilitates true single-supply operation with an input voltage as low as 2.2V.

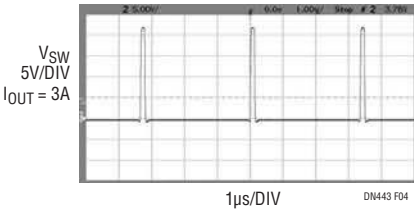

Figure 4. LT3740 Low Duty Cycle Waveforms

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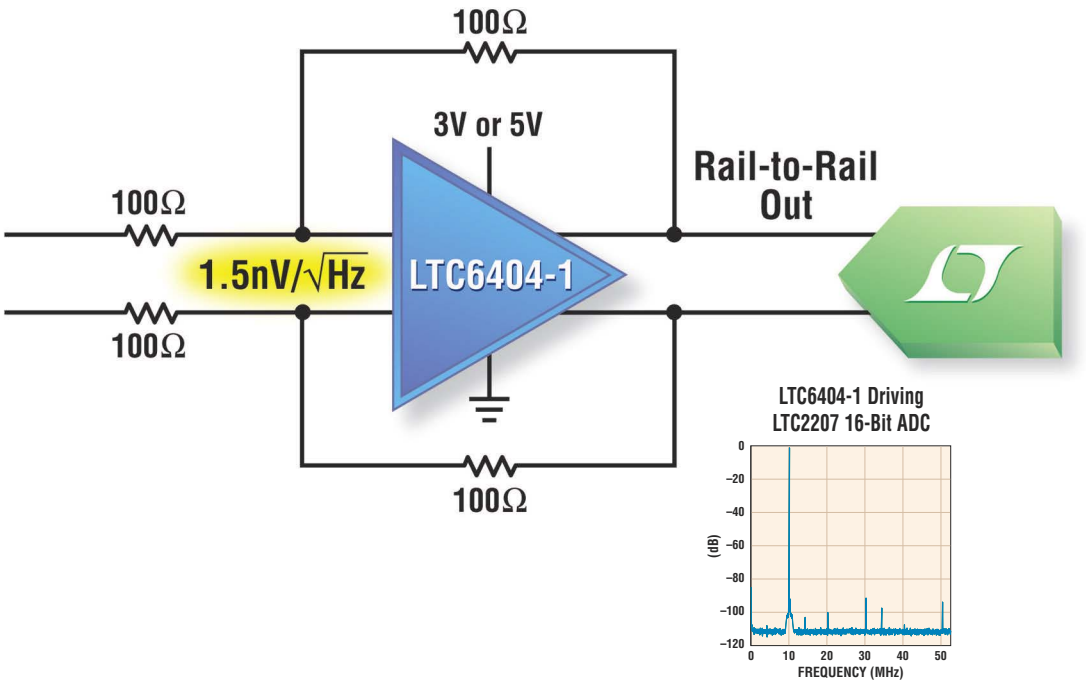

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Distortion	-95dBc @ 3MHz	-92dBc @ 10MHz	-72dBc @ 50MHz	-88dBc @ 70MHz	-81dBc @ 140MHz
Noise	2.8nV/√Hz	1.5nV/√Hz	1.6nV/√Hz	2.1nV/√Hz	2.1nV/√Hz
Supply Voltage	2.7V to 5.25V	2.7V to 5.25V	2.7V to 3.5V	2.85V to 3.5V	2.85V to 5.25V
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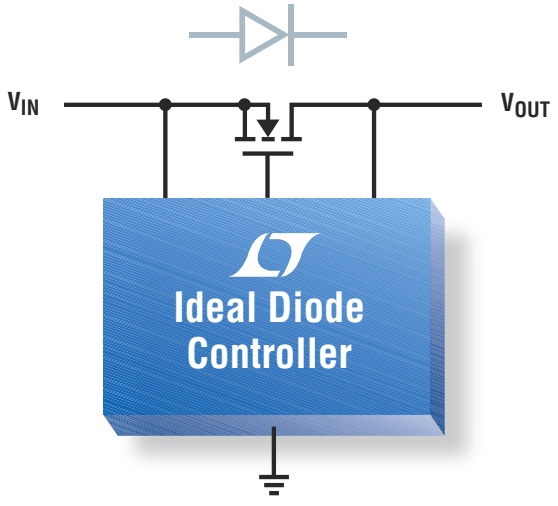

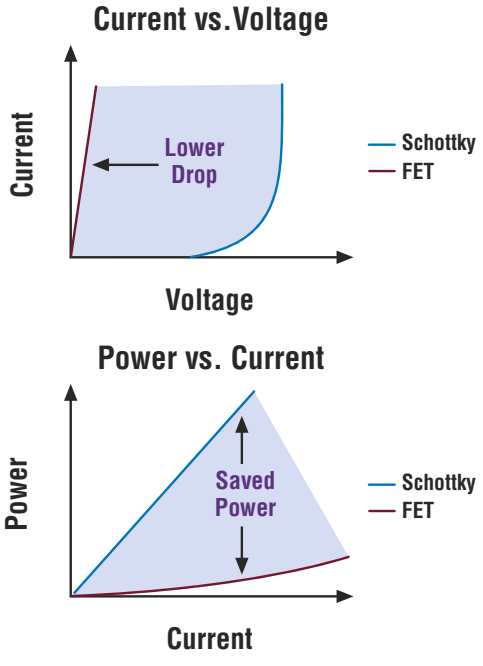

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LTC4355	9V to 80V	Dual	Yes	3 x 4 DFN-14, SO-16	
LTC4357	9V to 80V	Single	No	2 x 3 DFN-6, MSOP-8	
LT®4351	1.2V to 18V	Single	Yes	MSOP-10	

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READERS SOLVE DESIGN PROBLEMS

Precision temperature controller has thermal-gradient compensation

W Stephen Woodward, Chapel Hill, NC

Accurate and stable temperature control is necessary for effectively using many thermally sensitive components and sensors, such as semiconductor lasers and optical detectors. An industry has grown up in response to provide thermal-control devices, such as TECs (thermoelectric coolers), temperature sensors, and both monolithic and hybrid application-specific driver ICs, to facilitate the associated designs. This availability eases the implementation of high-performance thermostasis electronics with good dynamic behavior, because it allows you to assemble feedback loops with flexible and sophisticated control characteristics—PID (proportional-integral-differential) feedback loops, for example—with nothing more than appropriate choices of shunt resistance and capacitance. Unfortunately, achieving good static stability is sometimes more difficult because the thermal properties of a system, rather than the electronics, often cause limited temperature-control-loop static stability.

Every thermal-control system incurs nonzero thermal impedances in the heat-transfer paths between the source of heating, cooling, or both. These paths include the thermal load, which is the object of thermostasis; the temperature sensor—the thermistor, for example; and the ambient temperature. If the ratios of these impedances don't balance well, which, unfortunately, is usually the case, then

DIs Inside

70 Programmable current source requires no power supply

72 Pulse-width modulator has digital control

74 Microcontroller controls analog phase shifter

74 Composite instrumentation amplifier challenges single-chip device for bandwidth, offset, and noise

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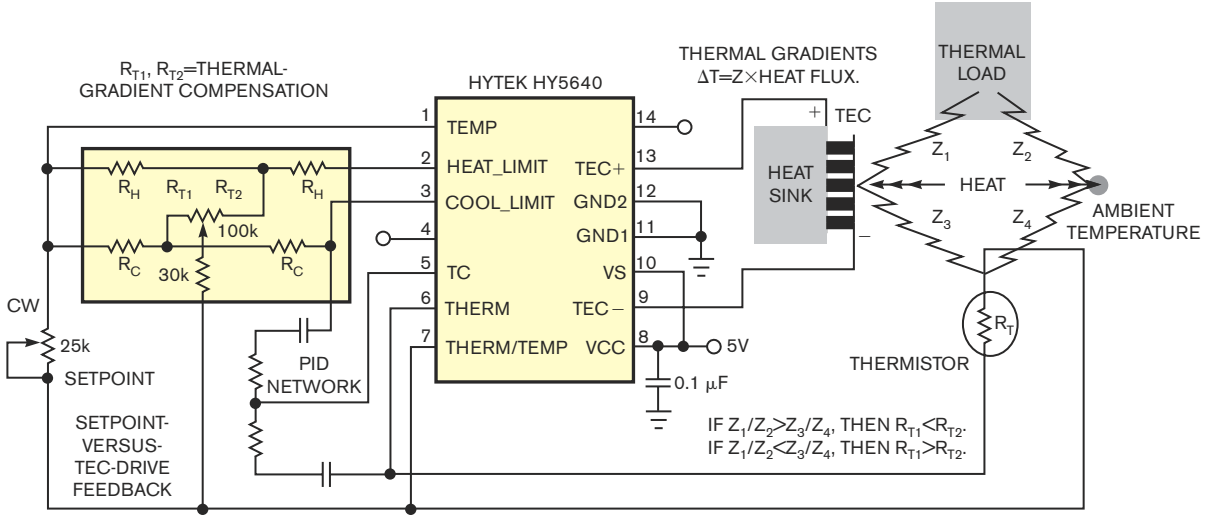

Figure 1 This circuit partially cancels the effects of thermal gradients in the load's thermal impedances. It works by providing an adjustable positive- or negative-feedback path from the TEC-drive level that couples changes in ambient temperature into compensating changes in the thermistor setpoint.

even perfect thermostasis of the sensor doesn't equate to adequate stability of the load's temperature (**Figure 1**).

For example, if Z_1/Z_2 is greater than Z_3/Z_4, where Z is the impedance, then rising ambient temperatures will cause the temperature of the load to rise, whereas falling ambient temperatures will cool the load. By contrast, if Z_1/Z_2 is less than Z_3/Z_4, then rising ambient temperatures will cause the temperature of the load to fall and vice versa (**Figure 2**). Reducing the parasitic impedances with tighter thermal coupling and better insulation can reduce but seldom eliminate the gradient and magnitude of the error.

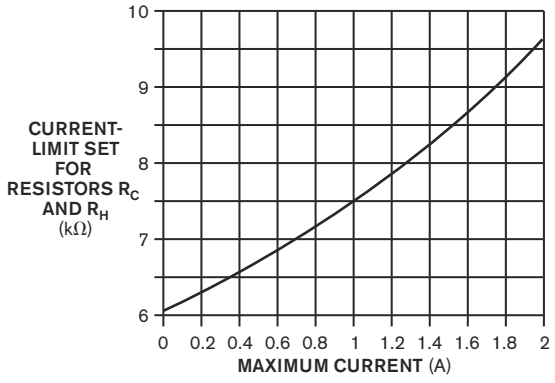

Figure 2 The TEC's maximum-drive heat- and cool-current ratings determine the selection of current-sampling resistors R_C and R_H.

The circuit in **Figure 1** provides a different solution: an electronic workaround to at least partially cancel the effects of thermal gradients in the impedances. It works by providing an adjustable positive- or negative-feedback path from the TEC-drive level that couples changes in ambient temperature and, therefore, in TEC drive into compensating changes in the thermistor-setpoint temperature. The implementation in **Figure 1** uses a popular hybrid TEC controller. Two signal nodes that track TEC drive, COOL_LIMIT and HEAT_LIMIT, are inputs to an adjustable bridge circuit that comprises R_{T1}, R_{T2}, the potentiometer, and associated circuitry. With correct adjustment of R_{T1} and R_{T2}, a test determined that the thermistor setpoint must move either with or in opposition to ambient temperature, so that net stability of the load results. A version of this concept flew as part of two tunable-diode laser spectrometers in the science package of the 1999 Mars Polar Lander (**Reference 1**).EDN

REFERENCE

1 May, Randy D, Siamak Forouhar, David Crisp, W Stephen Woodward, David A Paige, Asmin Pathare, and William V Boynton, "The MVACS tunable diode laser spectrometers," American Geophysical Union, *Journal of Geophysical Research*, Volume 106 (E8), 2001, pg 17,673, www.agu.org/pubs/#journals.

Programmable current source requires no power supply

John Guy, National Semiconductor, Santa Clara, CA

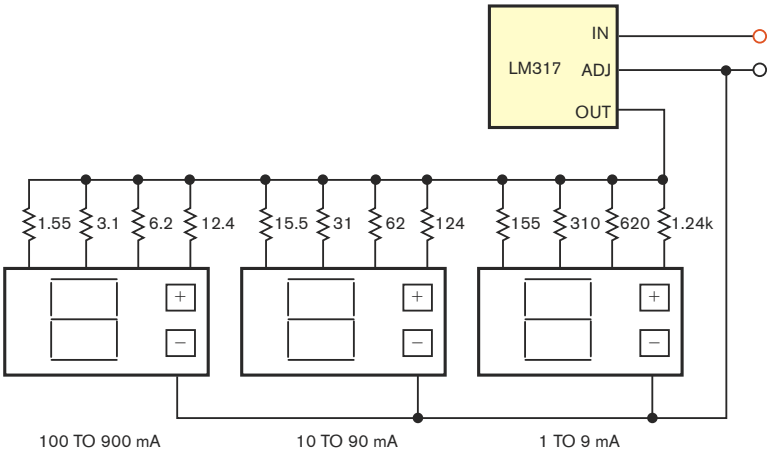

Figure 1 This programmable current source uses BCD switches to set the current limit.

Engineering labs are usually equipped with various power supplies, voltmeters, function generators, and oscilloscopes. One piece of equipment missing from many such labs, however, is a current source. This omission is unfortunate, because a current source is useful for creating I-V (current-versus-voltage) curves, charging and discharging batteries, preloading power supplies, and many other applications.

The circuit in **Figure 1** is an easy-to-build, easy-to-use, low-cost current source. It comprises three sections of BCD (binary-coded-decimal) switches, a three-terminal adjustable regulator, a handful of 1%-tolerant resistors, and a National Semiconductor (www.national.com) LM317 three-terminal adjustable regulator. All newer National Semiconductor regulators are of the low-dropout type, which is unsuitable for this application. The switches short their four outputs to a common terminal based

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LT3474/-1	Buck	400:1 PWM	4 to 36	9/25	1.00	TSSOP-16E
LT3475/-1	Dual Buck	3000:1 PWM	4 to 36 (40 Max.)	9/25	1.50 x 2	TSSOP-20E
LT3476	Quad Buck, Boost, Buck/Boost Mode	1000:1 PWM	2.8 to 16	36	1.00 x 4	5mm x 7mm QFN-38
LT3477	Buck, Boost, Buck/Boost Mode	DC/PWM	2.5 to 25	40	2.00	4mm x 4mm QFN-20, TSSOP-20E
LT3478/-1	Buck, Boost, Buck/Boost Mode	3000:1 PWM	2.8 to 36 (40 Max.)	40	4.00	TSSOP-16E
LT3486	Dual Boost	1000:1 PWM	2.7 to 24	35	0.10 x 2	3mm x 5mm DFN-16
LT3496	Triple Buck, Boost, Buck/Boost Mode	3000:1 PWM	3 to 30 (40 Max.)	45	0.50 x 3	4mm x 5mm QFN-28
LT3517/18	Buck, Boost, Buck/Boost Mode	5000:1 PWM	3 to 30 (40 Max.)	45	1.0/2.0	4mm x 4mm QFN-16
LT3590	Buck Mode	200:1 PWM	4.5 to 55	n/a	0.05	2mm x 2mm DFN-6, SC-70
LT3595	Buck Mode	3000:1 PWM	4.5 to 45	n/a	0.05 x 16	5mm x 9mm QFN-56
LT3755/56	Buck, Boost, Buck/Boost Mode	3000:1 PWM	4.5 to 40/6 to 100	60/100	Ext. FET	3mm x 3mm QFN-16, MSOP-16E
LTC®3783	Buck, Boost, Buck/Boost Mode	3000:1 PWM	3 to 36	40	Ext. FET	4mm x 5mm DFN-16, TSSOP-16E

*Actual output current will depend on V_{IN}, V_{OUT} and topology.

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on the digit setting of the switch.

The circuit operates as follows: Assume that the red terminal in **Figure 1** connects to a 5V power supply and that the black terminal connects to the power supply's ground. Assume that the middle digit (labeled 10 to 90 mA) gets set to two and that the other two digits get set to zero. The BCD switch connects a 62Ω resistor from the LM317's output to adjust pins. The LM317 forces 1.25V across the 62Ω resistor, causing 20 mA to flow from the output pin through the resistor, and to the black terminal of the current source. The circuit maintains this regulation provided that the input voltage remains 3 to 40V.

To construct the current source, you should either use a heat sink for the LM317 or build the circuit into a die-cast aluminum housing, which acts as the heat sink. Isolate the LM317 from the heat sink using a thermally conductive isolation pad and a shoulder washer. You determine the resistors' values by starting with the base-resistance value, 1.24 kΩ. Then, simply use parallel values to determine the successive resistors' values. For example, two 1.24-kΩ resistors in parallel yield 620Ω, four 1.24-kΩ resistors in parallel yield 310Ω, and so on. Using this approach with ¼W resistors ensures that the highest current resistors do not overheat. For example, eight 12.4Ω, ¼W resistors yield 1.55Ω resistance and dissipate only 1W with a peak capability of 2W.

The performance of the circuit is about 2% accurate. You can achieve higher accuracy with hand-selected resistors. The output impedance for lower currents is more than 1 MΩ but drops to approximately 250 kΩ at 200 mA. EDN

Pulse-width modulator has digital control

S Vinay Kumar, Mysore, India

In this Design Idea, the total time period of an output pulse's width is 16 times the pulse width of the input clock. The input clock connects to a binary counter (**Figure 1**). The output of the binary counter then goes to a decoder. The decoder scans the signal such that the first output of the decoder goes to an inverter gate and then to the counter. The output of the counter then goes to one as soon as the signal to the counter goes from zero to one and then from one to zero.

The multiplexer decodes the output pulse width's time to be in the on state. The first output of the demultiplexer sets the output of the counter, and the next outputs clear the output of the counter. The multiplexer, a 14067, selects the clearing signal. Upon the 0th input of the multiplexer, the PWM (pulse-width-modulator) output becomes zero because the setting time and clearing time become nearly zero. The last input of the multiplexer does not connect, so the final input selection becomes independent of the PWM output. The design uses all the intermediate input selections of the multiplexer. EDN

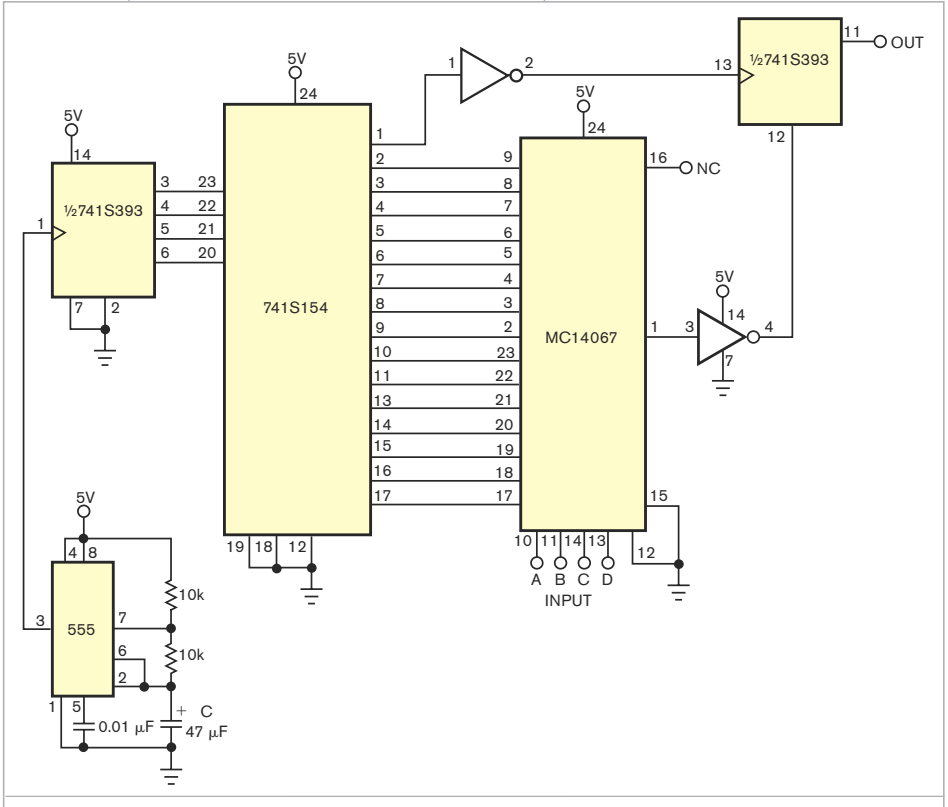

Figure 1 In this digitally controlled pulse-width modulator, the period of the output is 16 times the pulse width of the input clock.

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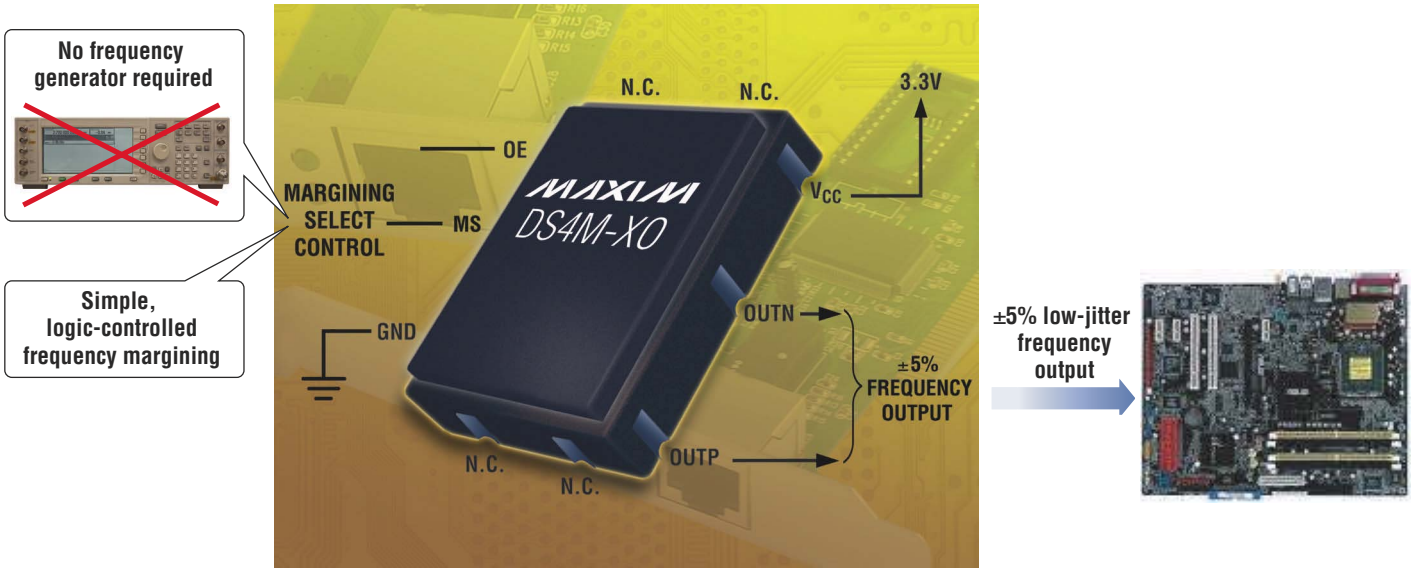

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Microcontroller controls analog phase shifter

Nick Ierfino, IGS Technologies, Montreal, PQ, Canada

Phase shifters find use in a variety of circuits, but variation in amplifier and capacitance tolerances usually makes it difficult to control the exact phase shift that precise control circuitry requires. The circuit in **Figure 1** can control the phase shift from input to output by using IC_3, an AD5227 64-step-up/step-down control digital potentiometer, to replace the value for the resistance. The formula of the center frequency of the output is $1/(2\times\pi\times R\times C)$. Different ranges of resistance are available for the AD5227. This example uses a 10-kΩ value. By stepping through the 64 points, the 720-kHz input sine wave rotates several times from 0 to 360°. The AD5227 acts as a potentiometer, in which A and B are the extremes and W is the wiper.

This example uses IC_2, a PIC16F84 microcontroller with a crystal frequency of 20 MHz. This microcontroller has a theoretical potential performance of 5 MIPS and should serve many purposes in PLL (phase-locked-loop) circuitry. You could use any microcontroller or even an FPGA to control the AD5227. EDN

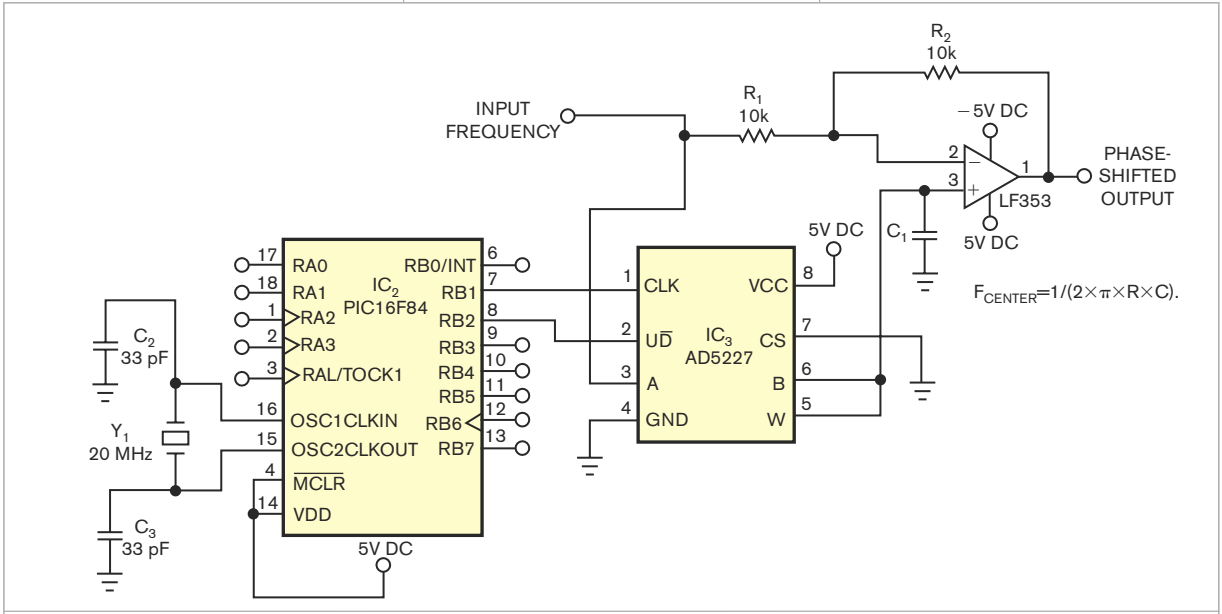

Figure 1 A PIC16F84 sets the resistance of the AD5227 digital potentiometer, precisely controlling the phase shift of the output with respect to the analog input.

Composite instrumentation amplifier challenges single-chip device for bandwidth, offset, and noise

Marián Štofka, Slovak University of Technology, Bratislava, Slovakia

Although the prevailing number set in electronics is binary, human-machine interaction uses a decimal-number set. For this reason, designs often require the use of amplifiers with gain programmable in steps in the power of 10. Currently, Analog Devices' (www.analog.com)AD8253 monolithic instrumentation amplifier is digitally programmable with voltage gains of one, 10, 100, and 1000 (**Reference 1**). This IC has high bandwidth at lower gains, but you inevitably sacrifice this bandwidth when the amplifier has a gain of 1000. If your application's demands for bandwidth reach the megahertz range at a gain of 1000 and if offset and noise performance prevail over circuit complexity, then a composite amplifier may fill the bill (**Figure 1**).

The composite amplifier is a cascade of three Analog Devices' AD8250 digitally gain-programmable amplifiers IC_1, IC_2, and IC_3 (**Reference 2**). The AD8250 is programmable for voltage gains of one, two, five, and 10. Because the gains of one and 10 are the only

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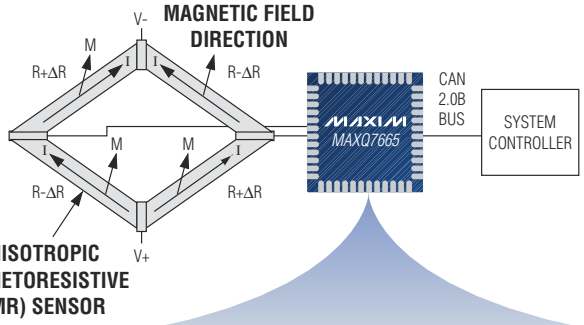

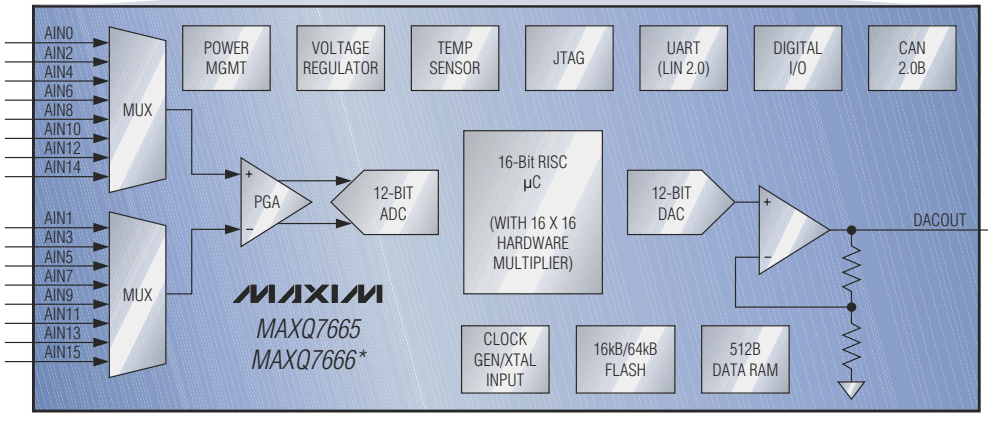

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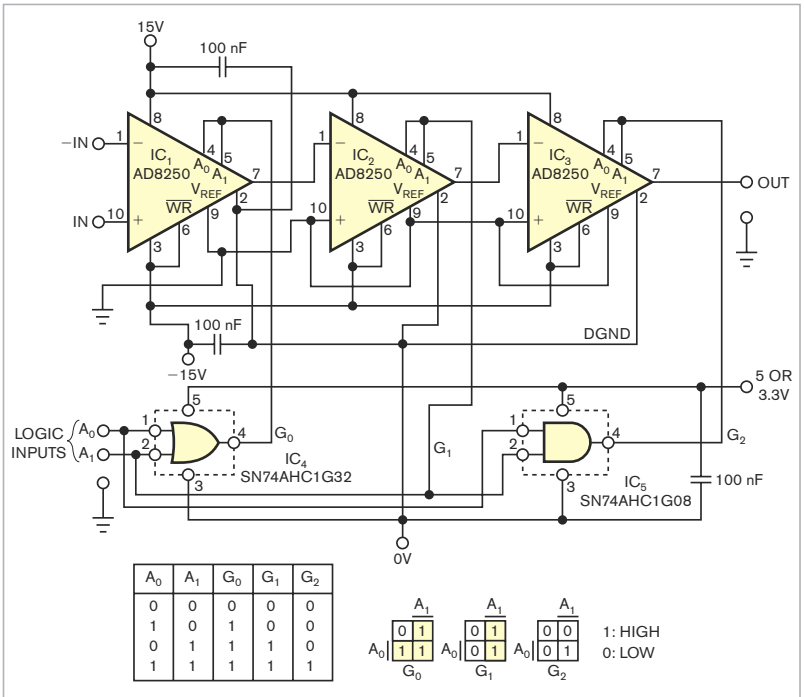
ones of interest in this case, the 2-bit words corresponding to these two values of gain are the zero and three in binary code, and the two logic pins of each of these three ICs connect. The AD8250 has a typical bandwidth of 3.8 MHz and a guaranteed bandwidth of 3 MHz at a gain of 10. The net result is that the bandwidth of the amplifier is 1.9 MHz at a gain of 1000, which is more than six times that of the single-chip AD8253. The low-frequency noise is less than 40% of that of the single-chip device. EDN

REFERENCES

1 "AD8253 10 MHz, 20V/µs, G=1, 10, 100, 1000 iCMOS Programmable Gain Instrumentation Amplifier," Analog Devices, 2007, www.analog.com/pr/AD8253.

2 "AD8250 10 MHz, 20V/µs, G=1, 2, 5, 10 iCMOS Programmable Gain Instrumentation Amplifier," Analog Devices, 2007, www.analog.com/pr/AD8250.



A_0	A_1	G_0	G_1	G_2
0	0	0	0	0
1	0	1	0	0
0	1	1	1	0
1	1	1	1	1

Figure 1 Although comprising five IC packages, this digitally gain-programmable instrumentation amplifier reaches a typical bandwidth of 1.9 MHz at a gain of 1000 and thus covers the megahertz range at any of the programmable gains of one, 10, 100, and 1000.

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ABM Drives Inc, www.abm-drives.com

Controller IC targets three-phase motors

Targeting use in automotive Hall-commutated three-phase motors, the temperature- and voltage-grade A3930 and A3931 three-phase BLDC (brushless-direct-current)-motor-controller ICs integrate the commutation logic onboard. The microprocessor directly drives the Hall-sensor inputs, making the devices suitable for automotive-grade ICs for robust BEMF (back-electromotive-force) sensorless devices. An on-chip commutation decoder and state machine read the inputs of three Hall-sensor or I/O inputs from the processor and then output the gate-drive signals controlling three high-side and three low-side discrete external NMOS MOSFETs that drive the three-phase BLDC motor. Additional features in-

MOTION

clude an integrated charge pump, a 5.5 to 50V battery-voltage range, extensive diagnostics, a low-current quiescent-current mode, and a 5V supply requiring an external NPN transistor for the Hall sensors. Available in a 48L eLQFP package, the A3930 and A3931 controller ICs cost $3.12 (1000) each.
Allegro MicroSystems, www.allegromicro.com

PLCopen-compliant software allows for programming in five additional languages

Version 6.0 of the vendor's motion-control-application-development kit provides PLCopen-compliant control software, allowing users to program in five languages, in addition to ACSPL (ACS programming language)+. The software provides variable mapping, enabling flexible bidirectional interfacing, mutual synchronization, and functionality exchange between ACSPL+ and IEC (International Electrotechnical Commission) 61131-3 programs. Additional features include CANopen (controller-area-network-open) support, allowing the configuration of SPiiPlus motion controllers as a CAN-open master, according to DS-402 specifications, as well as control of as many as 64 nodes of motion or I/O. The software provides a simulator tool for modeling a closed-loop servo system, enabling development of multiaxis controller programs in a PC environment with no motion-control hardware. An MMI (man-machine-interface) feature provides program and motion management, configuration, system analysis, servo turning, programming, parameter viewing, I/O monitoring, and safety tools. The free motion simulator is downloadable from the vendor's Web site.
ACS Motion Control, www.acsmotioncontrol.com

SRM-SPM power modules suit small-motor applications

Driving two-phase SRM (switch-reluctance-motor) designs in small-motor applications, the FCAS20DN60BB and the FCA30DN60BB SRM-SPM (smart power modules) combine 14 tested power components. The device integrates two high-voltage ICs, a low-voltage IC, four NPT (non-punch-through) IGBTs (insulated-gate bipolar transistors), four fast-recovery diodes, two bootstrap diodes, a thermistor, and several protection functions. Available in a 45×28-mm SIP package, the 600V, 20A FCAS20DN60BB and the 600V, 30A FCA30DN60BB cost $16.38 and $17.94 (100), respectively.
Fairchild Semiconductor, www.fairchildsemi.com

Development kit claims a 30% reduction of processor resources

Based on the STM32 flash microcontroller, the STM-3210B-McKit three-phase motor-control-development kit provides hardware and firmware for evaluating 32-bit devices or for beginning development of a sensorless-motor-control application. Using the ARM Cortex-M3 core, the device suits home-appliance and industrial applications. Using no sensors, the kit implements a vector-control algorithm for a three-phase PMSM (permanent-magnet-synchronous motor) in less than 25 μsec. This feature allows the device to use less than 30% of the processor's resources for most applications. The PMSM's code fits into less than 16 kbytes. Suiting use with PMSM and ac-induction motors, the hardware platform operates at 48V and includes schematics to reduce hardware-design time. The kit allows real-time control and monitoring using an onboard color LCD and joystick or stand-alone operation using an onboard pushbutton and trimmers. Additional features include the Segger J-Link USB-powered JTAG emulator and flash-programming and real-time-debugging capability. The STM3210B-McKit development kit costs $1129 with a 24V-dc PMSM.
STMicroelectronics, www.st.com

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BY STEPHEN TOMPOROWSKI • KAMAN MEASURING SYSTEMS

One giant leap for "enhanced" hybrid

In August 2002, I started a new job in an engineering department with 35-year-old products. I became the lead engineer on the flagship product, most of whose circuitry resided in a hybrid. The hybrid provider was not interested in our small quantities, and quality suffered. We submitted an "updated" design from one of the long-gone engineers to another hybrid house. At that point, there was no rush, and we had plenty of stock.

A wonderful application then emerged. A major contractor wanted our product to go into space. We had a military-qualified hybrid, so it was only "one small step" to an aerospace application, or so we thought. The new hybrid house had all the expertise we required, and the project was now suddenly in overdrive.

But then the hybrid tech called me and said that the internal oscillator was working but wasn't displaying a sine wave. I asked what it was displaying, but he couldn't explain it.

This eddy-current-measurement system had a combined oscillator/AGC (automatic-gain-control) system for a stable signal to the sensor. This technique involves the use of two intertwined loops: one feedback for the crystal oscillator and another to control the amplitude.

The next week, bearing the schematics of both the old and the new hybrids, I drove five hours to the hybrid house. The tech showed me the output of the oscillator. I couldn't describe the signal, either. It periodically spiked, curved, and jumped. As I puzzled over that situation, the tech brought his bench magnifying lamp close to the circuit, and bang! A perfect sine wave appeared. Because the hybrid was using bare dice, the proximity of the light probably changed the gain of the differential amplifier. I shrugged it off as a neat parlor trick and dug into the circuitry.

The first thing I noticed was that the schematic had an emitter resistor on the gain transistor twice the size of the resistor in the old circuit. Fiddling with that problem, we found that we had to reduce the emitter resistance to almost zero to get a good sine wave. That approach didn't sit well with me because it wouldn't give the collector current much limiting. Going back to the output of the differential amp, I noticed that the ugly signal was much higher in amplitude than the oscillator output should be and that it had shifted to positive. A clue! I traced the feedback for the amplitude and noticed that the system was rectifying only the negative swing of the signal and was using it for the error signal. With the signal shifted, there was no correction signal and the differential amp was running wide open. So, somewhere in that loop, something was amiss.

It turns out that someone had added some new circuitry at the output of the differential amp: a diode connected to a biased zener. When you start up any AGC system, you're bound to have a too-large signal due to the filter time constant on the error signal. It looked as if someone had tried to cut off the signal peaks from being too high until the AGC kicked in. But why did that person use a biased zener?

I had the tech remove the two components. Bingo! We saw a perfect sine wave. The attempt to limit the start-up amplitude was amiss in that someone had tried to place the limit on the wrong side of ground. The result was unique.

That hybrid design went into space and is about to do so again. The lesson? Beware of engineers bearing "enhancements"—that is, until you examine them first! EDN

Stephen Tomporowski is a design engineer at Kaman Measuring Systems (Middletown, CT). Like him, you can share your Tales from the Cube and receive $200. Contact edn.editor@reedbusiness.com.

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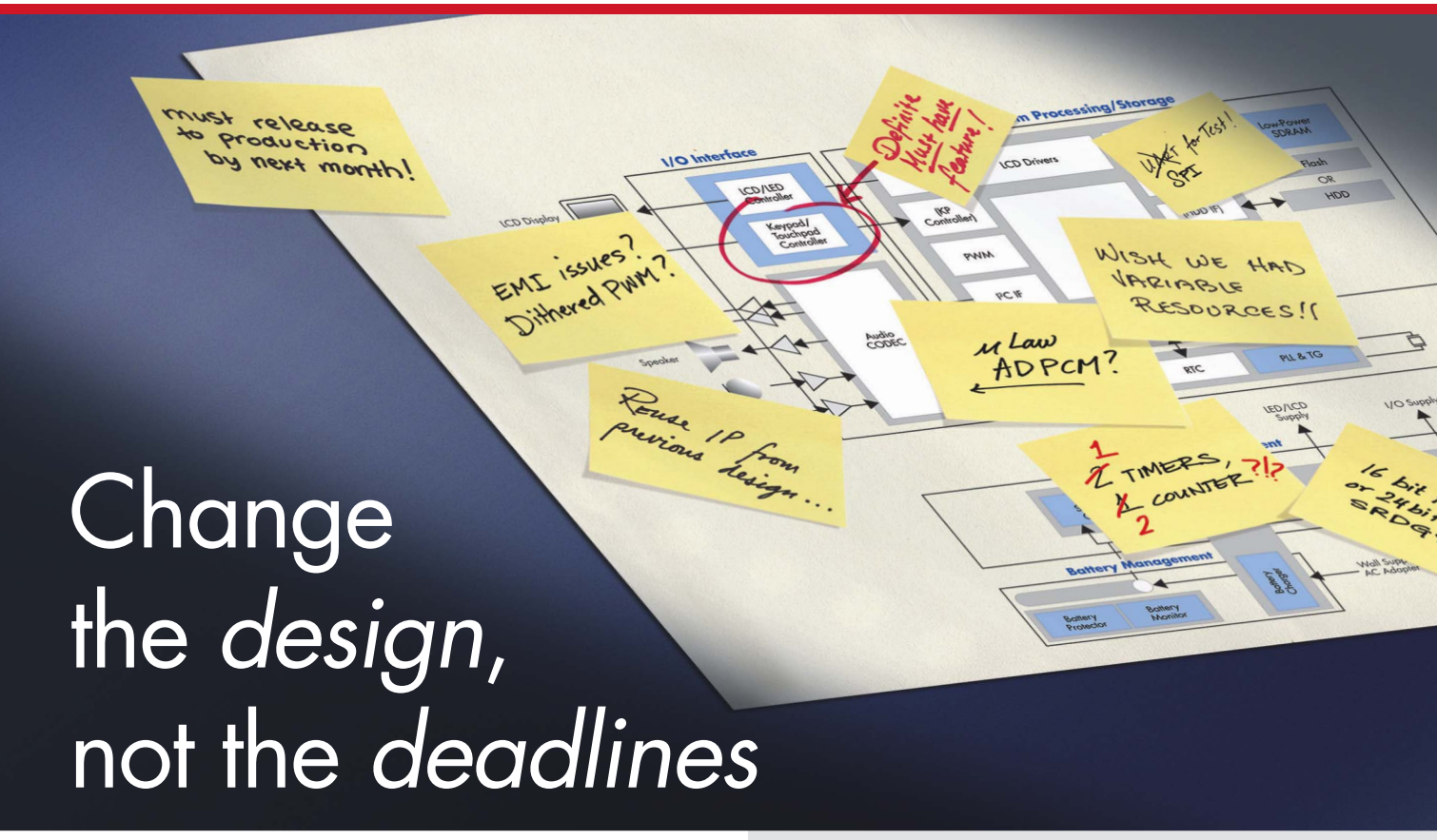

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- The configurability of an FPGA, the mixed-signal integration of an ASIC, and the familiarity of an MCU.
- Reusable IP, compatible device families and variable resource options so you can optimize design efforts and accommodate changes.
- Two powerful development platforms: PSoC Express™ Software for code-free visual embedded system design and PSoC Designer™ Software for complete flexibility to write code.

GET STARTED WITH PSoC NOW.

- *Download our "Change Happens" White Paper and get 50%* off a PSoC development kit:* **cypress.com/go/changepaper**
- *Download free PSoC Express™ or PSoC Designer™ embedded software:* **cypress.com/go/changesoft**
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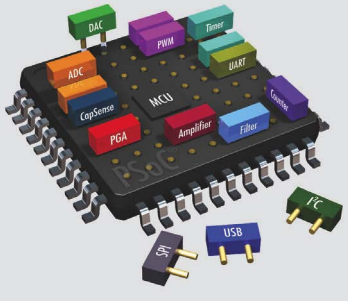

PSoC includes programmable analog and digital blocks, a fast MCU, flash and SRAM memory, all in a compact package (as small as 3mm x 3mm).

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*50% off applies to the PSoC Development Kit featured on www.cypress.com/go/changepaper.